

Study on switching behavior of silicon carbide MOSFET by gate driver

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Abstract. Compared with IGBT, SiC MOSFET has improved frequency efficiency, outstanding reliability which not only can achieve energy saving and loss reduction, but also increase power density and other characteristics. SiC MOSFETs are faced with countless challenges in practice because of their superior switching speed. The gate driver was adjusted in this paper to investigate the switching behavior of silicon carbide MOSFET. The switching behavior of silicon carbide devices was first characterized by simulation software using a double-pulse test bench. Different parasitic inductances, resistances and additional parameters were found to have significant impacts on SiC MOSFET switching behavior. The results are analysed after combination and comparison.

Keywords: IGBT, SiC MOSFET, gate driver, double pulse test, parasitic inductance.

1. Introduction

In the electronics manufacturing industry, power semiconductor devices, or power electronic devices are widely used. They can be applied in the fields of computers, communication, [1] modern energy, automobiles and others.

There are numerous advantages to using a comprehensive bandgap semiconductor device, including the fact that it has a larger energy-power bandgap which uses certain materials with a wide bandgap than silicon.

From the point of view of the parameters of the heating machine, it can achieve higher junction temperature, thin drift area, easier to adapt to a higher power, and so on [1].

The technology behind this type of device is relatively mature which has a promising future for technological advancements. It is a strong substitute for the previous Si technology compared with its SiC device in rated voltage, voltage drop, maximum temperature, thermal conductivity, and other values are relatively considerable [2], [3]. In addition, it can supplement Si's shortcomings in thermal capacity, voltage breakdown, and operating frequency. The latest generation of wide bandgap semiconductor devices can better meet the needs of aircraft, automobiles, and other industries and is a great substitute [4]. With the increase in the utilization rate of wideband gap devices in the power electronics industry, although they have advantages such as higher switching speed and overall loss reduction, they also face various challenges. For example, EMI is introduced into the process, significantly affecting the converter system. As a result of the short circuit of the bridge arm, in the half-bridge circuit, for example, noise from forward crosstalk will be produced. SiC MOSFET grids have poor voltage resistance, making them easy to damage, reducing their lifetime, or breaking their direct gate, causing negative crosstalk noise. In addition, elevated dv/dt also has adverse effects on motor winding insulation, which may accelerate the aging of insulators such as bonding wire and insulation rings [5], [6].

In some published papers discussing MOSFET behavior models, In [7] this paper presents a novel three-stage (3-L) AGD for trajectory control of SiC power MOSFETs, which has a unique shutdown delay advantage. On this basis, a comprehensive trajectory model is proposed for online model optimization of the interrupter, further verified on a double pulse test platform.

A high breakdown rate is attributed to the SiC MOSFET high-speed switch, intensifying the dv/dt effect, leading to a high breakdown rate [8]. We develop and optimize a gate driver to minimize gate inductance, eliminate negative bias breakdown and eliminate negative bias breakdown. Comparative study is verified in this experiment. In [9], an active grid driver (AGD) with an improved SiC

MOSFET switching path is proposed, which has been tested for high-frequency operation and the EMI and performance of AGDs. The final advantage of AGD is that it can reduce oscillation and overshoot losses without affecting the EMI performance. Power supply for SiC MOSFETs with an asymmetric power supply is possible with this device.

A double pulse test device was developed using the LTspice model. The behavior of the SiC MOSFET was investigated comprehensively under a variety of gate driving signals.

2. Introduction to switch behavior locus

Two types of losses are associated with power semiconductor devices: switching loss and conduction loss. MOSFETs and diodes typically have straightforward calculations for their conduction losses.

The static I-V characteristic is used to calculate the device conduction loss. As a result, this paper will focus on switching losses.

To quantify the switching losses of power semiconductor devices, an analytical power loss model is proposed based on the switching waveforms. The analog circuit for inductive switching of a SiC Schottky diode and a SiC MOSFET is shown in Fig. 1 to calculate the switching loss [10]–[12].

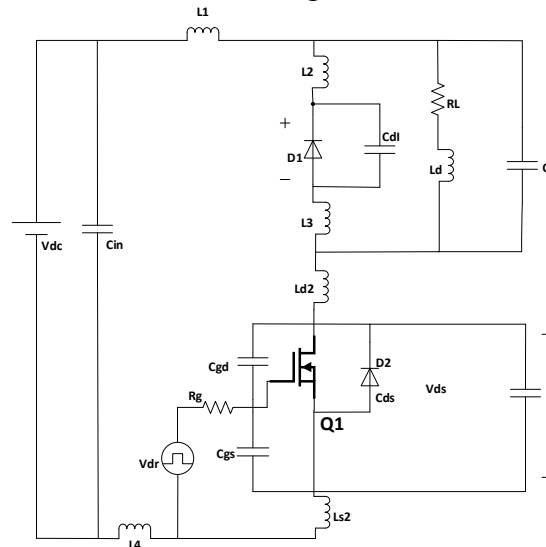


Fig. 1 Equivalent circuit of double pulse test. [13]

SiC MOSFET Q1 appears in this circuit, Schottky diode D2 is internal to the MOSFET, and SiC Schottky diode D1 is external to the MOSFET. During MOSFET switching, a DC voltage source V_{dc} is connected to a large inductor L_d , with a constant load current I_o . There is an assumption that the gate signal of Q1 commutates between V_{dr_L} and V_{dr} . The gate typically receives a positive voltage (15V–20V) during turn-on and a slightly negative voltage (-5V–2V) at turn-off. To reduce conduction losses due to their modest transconductance, SiC MOSFETs are typically operated at some positive voltage of at least 18V. A parasitic inductance is extracted from a device's package and PCB. It includes L_1 , L_2 , L_3 , L_{d2} , L_{s2} and L_4 . In MOSFETs, gateway-source capacitances C_{gs} , gate-drain capacitances C_{gd} , and drain-source capacitances C_{ds} serve as parasitic elements. As can be seen in Fig.2 [13], C_{gd} and C_{ds} exhibit a stepwise characteristic with two different values as a function of drain-source voltage. When V_{ds} is greater than $V_{gs} - V_{th}$, $C_{gd} = C_{gd1}$ and $C_{ds} = C_{ds1}$. V_{ds} equals or is less than $V_{gs} - V_{th}$, C_{gd} equals C_{gd2} , and C_{ds} equals C_{ds2} . A load inductor has an equivalent parallel capacitance C_L , while a Schottky diode has an equivalent junction capacitance C_{d1} . R_L is the DC resistance of the load inductor.

Fig.3 shows the critical waveforms during the turn-off. The fundamental waveforms during the turn-on are shown in Fig.4. The gate driver output voltage V_{dr} is shown in these figures. The gate-source voltage V_{gs} is shown in these figures, too. During drain current in a SiC MOSFET, V_{ds}

represent drain-source voltage, I_{ds} represent drain current. A SiC MOSFET's channel current is represented by I , a SiC Schottky diode is represented by I_{diode} . A SiC Schottky diode's cathode-anode voltage is represented by V_{diode} . Power semiconductor devices are capable of switching over several time intervals, depending on their physical behavior. A loss model is below to derive how loss is calculated for turn-ons and turn-offs.

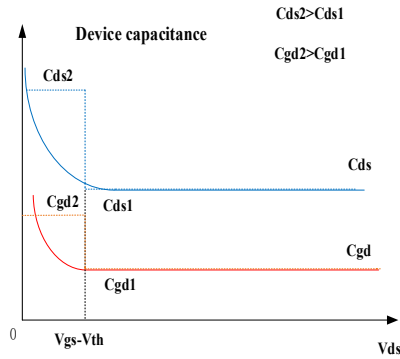


Fig. 2 Based on V_{ds} , the nonlinear capacitance C_{ds} and C_{gd} are plotted

2.1 Turn-on of MOSFETs

Because the inductive load is at its highest current at t_0 when the Schottky diode D1 is carrying the entire draft, a switch transition occurs. As a result the voltage drop across the Schottky diode D1 and the DC input voltage to the MOSFET, a voltage drop is observed across the drain and source of the SiC MOSFETs. When both sources and drains are off simultaneously, V_{dc} plus V_d is the voltage across them. As shown in Fig. 3, the waveforms of the turn-on switching have been schematically shown. The next section will examine these waveforms in more detail.

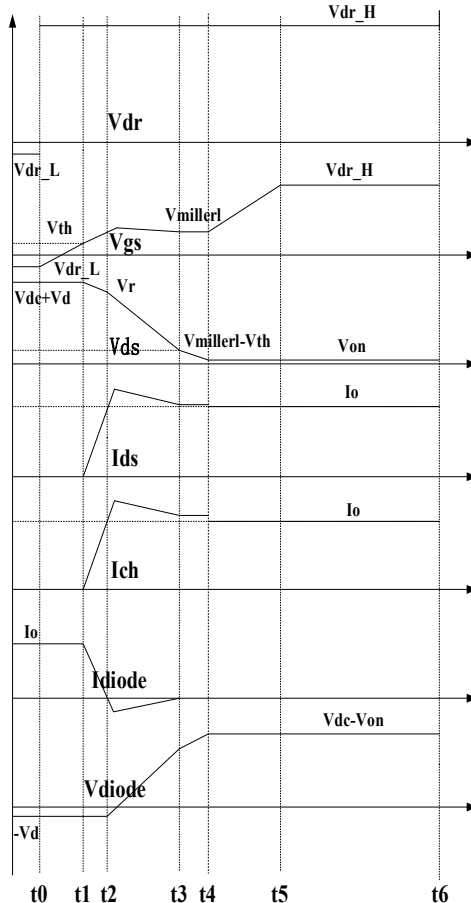


Fig. 3 Transition key waveforms for MOSFET turn-on [12]

Stage 1 [t0-t1] turn-on delay time: The gate signal Vdr is switched from Vdr_L to Vdr_H at time t0. For the MOSFET to turn on, it must reach its threshold voltage, Vth, at time t1. There is still a current flowing through Schottky diode D1 in SiC.

Stage 2 [t1-t2] current rise Phase: The drain current Ids reach the inductive load current Io as the voltage Vgs exceeds the voltage Vth. Because of the high di/dt ratio, the drain-source voltage decreases in this part of the circuit because of the parasitic inductance voltage drop. Schottky diode D1 currently has a zero current flow at time t2. Drain current is determined by:

$$I_{ds}(t) = g_{fs}[v_{gs}(t) - V_{th}] \quad (1)$$

where gfs is the trans-conductance of the SiC MOSFET. This period has the following duration:

$$t_2 - t_1 = \frac{C_{iss}(V_{miller1} - V_{th})}{I_{g2}} = \frac{I_o C_{iss}}{g_{fs} I_{g2}} \quad (2)$$

A gate driver's average current Ig2 in stage 2 equals the sum of Cgs + Cgd1, and a load's inductive current Io equals the inductive load current. The average gate driver's current Ig2 is calculated as follows:

$$I_{g2} = \frac{V_{dr_H} \cdot 0.5(V_{miller1} + V_{th}) \cdot \frac{L_{s2} I_o}{t_2 \cdot t_1}}{R_g} \quad (3)$$

The period t2-t1 can be calculated using formulas (3) and formula (2), as shown here.

$$t_2 - t_1 = \frac{\frac{C_{iss} R_g I_o}{V_{dr_H} - 0.5V_{th} - 0.5V_{miller1}} + L_{s2} I_o}{g_{fs}} \quad (4)$$

As a result of stray inductance in loop LS (=L1+L2+L3+L4+Ld2+Ls2), the MOSFET drain-source voltage drops:

$$V_{ds}(t) = V_{dc} + V_d - L_s \frac{di_{ds}}{dt} \quad (5)$$

MOSFET drain-source voltage Vds(t2) = Vr at t=t2.

$$V_{ds}(t_2) = V_r = V_{dc} + V_d - L_s \frac{I_o}{(t_2 - t_1)} \quad (6)$$

During this period [t1, t2], there was a total switching energy loss of:

$$\frac{3(t_2 - t_1)(V_{dc} + V_d) - 2I_o^2 L_s}{6} \quad (7)$$

Stage 3 [t2-t3] current rise Phase: voltage fall time I: When time t2 arrives, the SiC MOSFET takes over the total inductive load current and discharges the Coss output capacitance. In this period, MOSFET drain-source voltages decrease. SiC Schottky diodes are almost immune to reverse recovery effects because of their junction capacitance. The reverse capacitive current in MOSFETs causes additional switching losses. As a result, it reaches the boundary voltage Vmiller1-Vth at time t3. The drain-source voltage Vds in stage 3 [t2-t3] decreases with a steep slope dv/dt, as follows:

$$\frac{dV_{ds}}{dt} = -\frac{I_{g3}}{C_{gd}} = \frac{V_{miller1} - V_{th} - V_r}{t_3 - t_2} \quad (8)$$

A gate-drain capacitance is Cgd, and a gate-drain capacitance is Cgd1.

$$t_3 - t_2 = \frac{(-V_{miller1} + V_{th} + V_r) C_{gd}}{I_{g3}} \quad (9)$$

The gate drain capacitance $C_{gd} = C_{gd1}$.

The following losses have been measured for this period, including voltage current overlap loss as well as capacitance charging failure:

$$E_{2_3} = \int_{t_2}^{t_3} I_{ds} V_{ds} = \frac{(t_3 - t_2)(V_r + V_{miller1} - V_{th})}{2} (I_o + 0.5(C_{d1} + C_L)(V_{dc} + V_d - V_{miller1} + V_{th})) (V_r + V_{miller1} - V_{th}) \quad (10)$$

As shown in this example, C_{d1} is equivalent to the capacitance of a Schottky diode, and C_L is equal to the parallel capacitance of a load inductor.

Stage 4 [t3-t4] voltage fall time II: At time t3, the SiC MOSFET enters the ohmic region. Measurement of gate-drain and drain-source capacitance takes place with ohmic capacitances C_{gd2} and C_{ds2} . A V_{on} voltage drop occurs when a MOSFET is on. Until the on-state voltage V_{on} is reached, the drain-source voltage V_{ds} must remain low.

A decreasing slope dv/dt is associated with a decrease in the drain-source voltage V_{ds} throughout stage 4 [t3, t4], saying:

$$\frac{dV_{ds}}{dt} = -\frac{I_{g4}}{C_{gd}} = \frac{V_{on} - V_{miller1} + V_{th}}{t_4 - t_3} \quad (11)$$

A gate-drain capacitance C_{gd} is equal to a gate-drain capacitance C_{gd2} .

It is estimated that this period will last for the following amount of time [t3, t4]:

$$t_4 - t_3 = \frac{(V_{on} - V_{miller1} + V_{th})C_{gd}}{-I_{g4}} \quad (12)$$

A gate-drain capacitance C_{gd} is equal to a gate-drain capacitance C_{gd2} . Losses, including voltage-current overlap losses and capacitance charging losses, can be calculated as follows:

$$E_{3_4} = \int_{t_3}^{t_4} I_{ds} V_{ds} dt = \frac{(t_4 - t_3)(V_{miller1} - V_{th} + V_{on})}{2} (I_o + 0.5(C_{d1} + C_L)(V_{miller1} - V_{on} - V_{th})) (V_{miller1} + V_{on} - V_{th}) \quad (13)$$

C_{d1} represents the equivalent capacitance of a Schottky diode, while C_L represents the equivalent capacitance of a load inductor. When MOSFETs are in the on state, V_{on} represents the voltage drop.

Stage 5 [t4-t5] Remaining time for gate voltage rise: There is an exponential increase in gate-source voltage. The gate driver voltage reaches V_{dr_H} at time t5 when the gate-source voltage reaches the maximum gate driver voltage. During this period, there is no switching loss.

Stage 6 [t5-t6] MOSFET conduction time: The MOSFET handles inductive load current I_o . This is the period when MOSFETs suffer conduction losses.

2.2 Turn-off of MOSFETs

Inductive loads are controlled by SiC MOSFETs S , which carry the entire current I_o flowing through them. Schottky diode $D1$ is off. Voltages at the anode and cathode are $V_{dc} - V_{on}$, where V_{on} is the MOSFET S 's on-state voltage drop, and V_{dc} is its DC input voltage. The waveforms of typical turn-off switches are shown in Fig.4.

Stage 7 [t6-t7] turn-off delay time: In the region of ohmic resistance, the MOSFET operates at time t6, when Vdr_L is set as the gate signal. Once Vgs reaches Vmiller1, Vds will not increase. The gate driver circuit discharges the input capacitance Ciss.

Stage 8 [t7-t8] voltage rise time IAs a result, the MOSFET drain-source voltage Vds will increase during this period. MOSFETs are still operating in the ohmic region. At time t8, the drain-source voltage Vds transitions to the boundary voltage Vmiller1-Vth, and then the MOSFET transitions to saturation at the end of the period. Drain current Id and loading current Io should have an approximately equal relationship. Vds increases with a slope dv/dt in stage 8 [t7, t8], which is similar to:

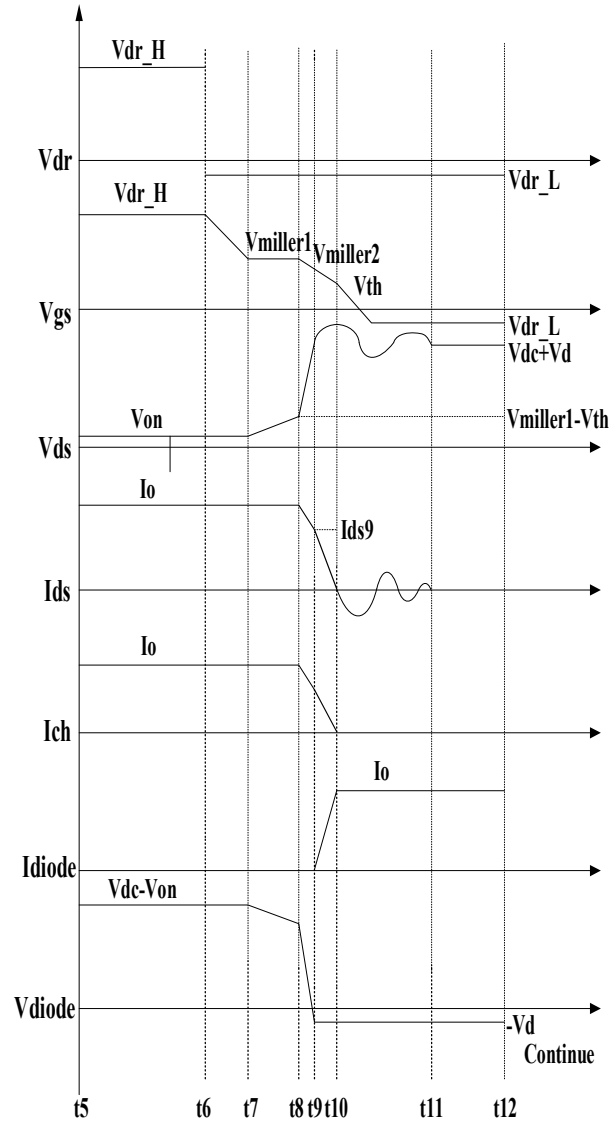


Fig. 4 Transition key waveforms for MOSFET turn-off [12]

$$\frac{dV_{ds}}{dt} = \frac{I_{g8}}{C_{gd}} = \frac{V_{miller1} - V_{th} - V_{on}}{t_8 - t_7} \quad (14)$$

where gate-drain capacitance $C_{gd} = C_{gd2}$.

This period [t7-t8] is estimated to last for the following time period:

$$t_8 - t_7 = \frac{(V_{miller1} - V_{th} - V_{on})C_{gd}}{I_{g8}} \quad (15)$$

The gate-drain capacitance $C_{gd} = C_{gd2}$.

Based on period $[t_7-t_8]$, the measured total loss can be calculated as follows:

$$E_{7-8} = \int_{t_7}^{t_8} I_{ds} V_{ds} dt = I_o \frac{(t_8 - t_7)(V_{miller1} - V_{th} + V_{on})}{2} \quad (16)$$

The voltage drop across the MOSFET on-state is given by V_{on} .

Stage 9 $[t_8-t_9]$ voltage rise time II: This period is characterized by increased MOSFET drain-source voltage. When a load current is provided to a Schottky diode, the parallel capacitance C_L of the Schottky diode is discharged along with the junction capacitance C_{d1} . Charge currents C_{d1} and C_L reduce drain current from load current I_o .

A linear decrease in drain current I_{ds} occurs from I_o to I_{ds9} at time t_9 , and I_{ds9} can be calculated as follows:

$$I_{ds9} = I_o - (C_{d1} + C_L) \frac{dV_{ds}}{dt} = I_o - (C_{d1} + C_L) \frac{(V_{dc} - V_{miller1} + V_d + V_{th})}{(t_9 - t_8)} \quad (17)$$

$$I_{ch9} = I_{ds9} - (C_{gd} + C_{ds}) \frac{dV_{ds}}{dt} = I_{ds9} - (C_{gd} + C_{ds}) \frac{(V_{dc} - V_{miller1} + V_d + V_{th})}{(t_9 - t_8)} \quad (18)$$

The capacitance of gate-drain C_{gd} equals C_{gd1} , and the capacitance of drain-source C_{ds} equals C_{ds1} . In this period, V_{ds} have increased in slope as follows:

$$\frac{dV_{ds}}{dt} = \frac{I_{g9}}{C_{gd}} = \frac{V_{dc} + V_d - V_{miller1} + V_{th}}{t_9 - t_8} \quad (19)$$

where gate-drain capacitance $C_{gd} = C_{gd1}$.

In the time period $[t_8, t_9]$, the total switching loss is as follows:

$$E_{8-9} = \int_{t_8}^{t_9} I_{ds} V_{ds} dt = \frac{(t_9 - t_8)(V_{dc} + V_d - V_{miller1} + V_{th})}{2} (2I_{ds9} + I_o) + \frac{(t_9 - t_8)(V_{miller1} - V_{th})}{2} (I_{ds9} + I_o) \quad (20)$$

Here are the calculations for the duration of this period $[t_9, t_{10}]$:

Stage 10 $[t_9-t_{10}]$ Current fall time: At time t_9 , when Schottky diode $D1$ becomes forward-biased, it is observed that the current is diverted from MOSFETs to Schottky diodes. As soon as the drain current reaches zero, the interval ends.

When the gate-source voltage V_{gs} reaches V_{th} at time t_{10} , the MOSFET's channel current drops to zero. MOSFETs experience additional voltage stress when their drain current decreases due to voltage drops across parasitic inductors.

$$t_{10} - t_9 = \frac{I_{ds9} C_{iss}}{g_{fs} I_{g10}} \quad (21)$$

I_{g10} represents the average gate driver current in stage 10, and C_{gd1} indicates gate-drain capacitance at high drain-source voltage for MOSFET input capacitance $C_{iss} = C_{gs} + C_{gd1}$. The average I_{g10} of gate drivers during this period was:

$$I_{g10} = \frac{\frac{1}{2}(V_{miller2} + V_{th}) - V_{dr_L} - L_{s2} I_{ds9} / (t_{10} - t_9)}{R_g} \quad (22)$$

The value of L_{s2} is the inductance of the common source. the duration time $t_{10}-t_9$ is given by:

$$t_{10} - t_9 = \frac{R_g I_{ds9} C_{iss} + L_{s2} I_{ds9} g_{fs}}{(0.5V_{miller2} + 0.5V_{th} - V_{dr_L}) g_{fs}} \quad (23)$$

As a result of parasitic inductances flowing through the drain and source of the MOSFET, an inductive voltage drop occurs.

$$V_{ds}(t_{10}) = V_{dc} + V_d - L_s \frac{di_{ds}}{dt} = V_{dc} + V_d + L_s \frac{I_{ds9}}{(t_{10} - t_9)} \quad (24)$$

In the main circuit loop, L_s represents the stray inductance. During this period $[t_9-t_{10}]$, the switching loss was measured as follows:

$$E_{9_10} = \int_{t_9}^{t_{10}} I_{ds} V_{ds} dt = \frac{(t_{10} - t_9)(V_{dc} + V_d)}{2} \quad (25)$$

$$I_{ds9} + \frac{L_s I^2 ds9}{2}$$

Stage 11 $[t_{10}-t_{11}]$ voltage ringing time: MOSFET output capacitance and stray inductance are in resonance during this period, which produces drain-source voltage ringing. All of the ringing energy is subsequently dissipated by the stray resistance in the circuit, which subsequently damps the high-frequency resonance.

A measurement of ringing loss during a turn-off period $[t_{10}, t_{11}]$ is given by [11]:

$$E_{10_11} = 0.5Q_{peak} V_{peak} - 0.5Q_{Vdc} + V_d(V_{dc} + V_d) - V_{dc}(Q_{peak} - Q_{Vdc} + V_d) \quad (26)$$

In period $[t_{10}-t_{11}]$, V_{peak} is the drain-source peak voltage, Q_{peak} is the charge on the output capacitor when $ds=v_{peak}$, and $Q_{Vdc}+V_d$ represent the charge on the output capacitor when $ds=v_{dc}+v_d$.

Stage 12 $[t_{11}-t_{12}]$ Diode conduction time: Inductive load current I_o is conducted by diode D1. During the time period $[t_{11}, t_{12}]$, there are no switching losses.

3. Influence and Simulation Validation of Gate driver Driver on Switch Trajectory

As shown in [1] Fig. 5, a dual-pulse test bench is built using LTspice software, and its schematic diagram is shown in Fig. 1. Pulse gate driver is set in Fig. 5. The gate resistance is increased from 1 ohm to 30 ohms by adjusting the size of the gate resistance.

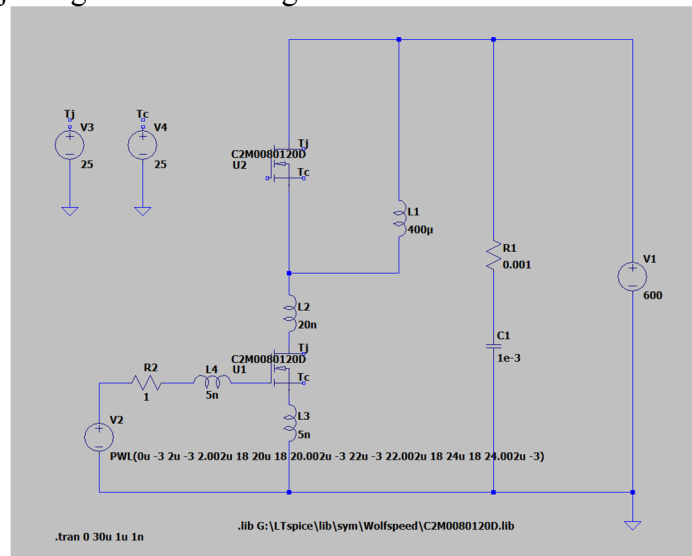
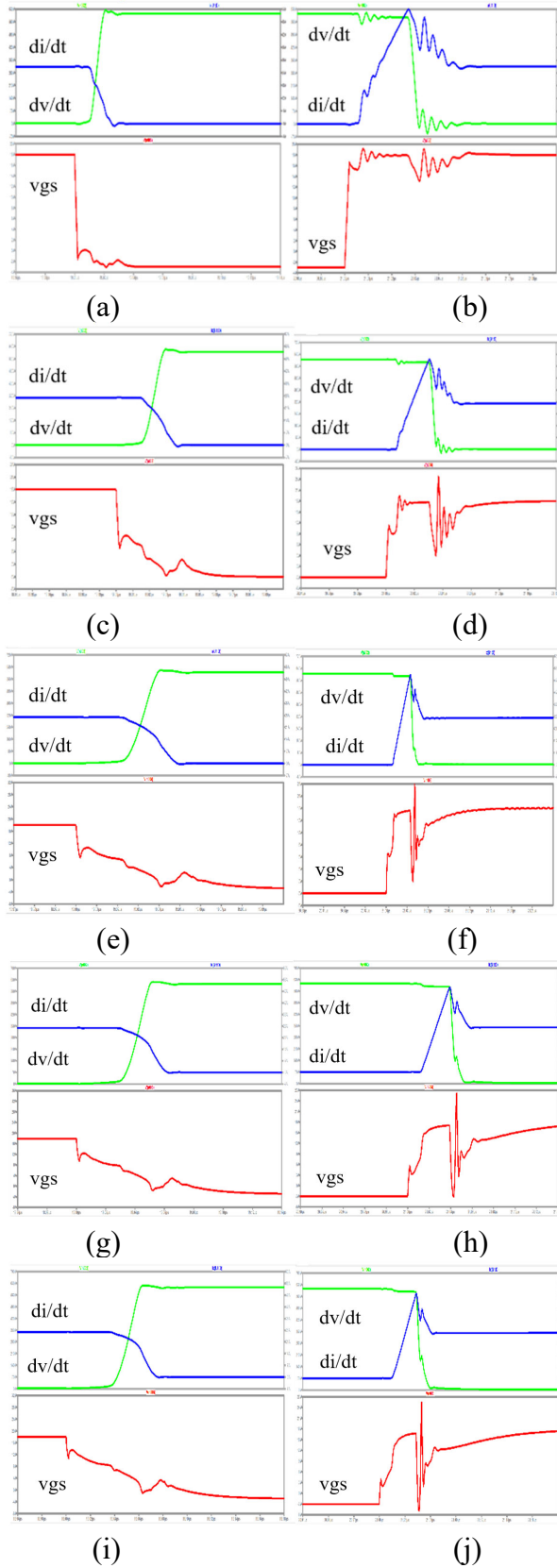


Fig. 5 Dual-pulse test bench built by LTspice

The simulation is performed every 50ohm, and the results are shown in Fig. 6.



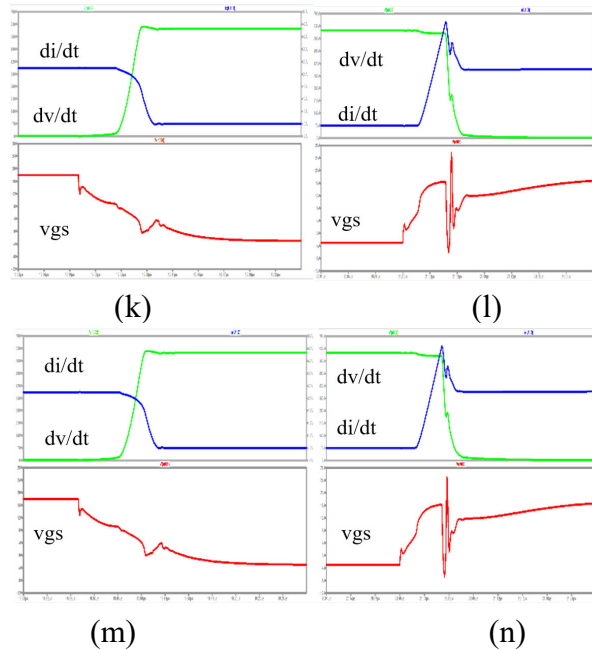


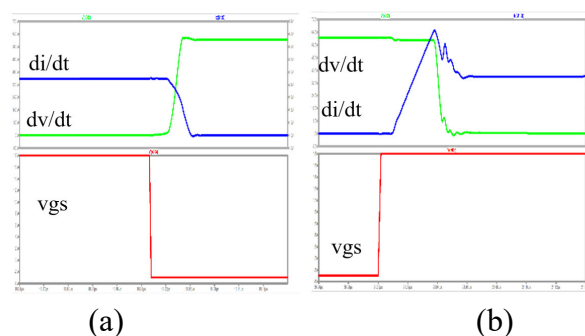
Fig. 6 A SiC MOSFET with different R_g is turned on and off. (a) Turn-off and (b) turn-on with $R_g = 1\Omega$, (c) turn-off and (d) turn-on with $R_g = 5\Omega$, (e) turn-off and (f) turn-on with $R_g = 10\Omega$, (g) turn-off and (h) turn-on with $R_g = 15\Omega$, (i) turn-off and (j) turn-on with $R_g = 20\Omega$, (k) turn-off and (l) turn-on with $R_g = 25\Omega$, (m) turn-off and (n) turn-on with $R_g = 30\Omega$.

Table 1. SiC MOSFETs switching slew rate with different R_G

$R_g(\Omega)$	dv/dt(V/ns)		di/dt(A/ns)	
	Turn off	Turn on	Turn off	Turn on
1	29.66	128.43	1.66	2.52
5	44.23	101.58	1.16	2.26
10	35.92	91.26	0.96	2.05
15	28.06	89.97	0.80	1.88
20	25.08	63.16	0.71	1.77
25	21.26	59.34	0.60	1.67
30	17.72	65.35	0.54	1.58

When R_g is equal to 1Ω , dv/dt turns off to $29.66V/ns$ and reaches the highest of $44.23V/ns$ at 5Ω . In the process of R_g from 5Ω to 30Ω , dv/dt decreases all the time. In the process of turn on, dv/dt decreases from 1Ω to 25Ω . There's an upward trend towards the last 30 . When R_g is equal to 1Ω , di/dt is $1.66A/ns$ in the turn off stage, and decreases in the middle stage, and also decreases with the increase of R_g in the turn on stage.

In Fig. 7, the influence of parasitic inductance will be tested, and the parasitic inductance values of drain and source will be adjusted to increase from a value of $1nH$ to a value of $50nH$, with simulations being conducted every $10nH$ during the simulation.



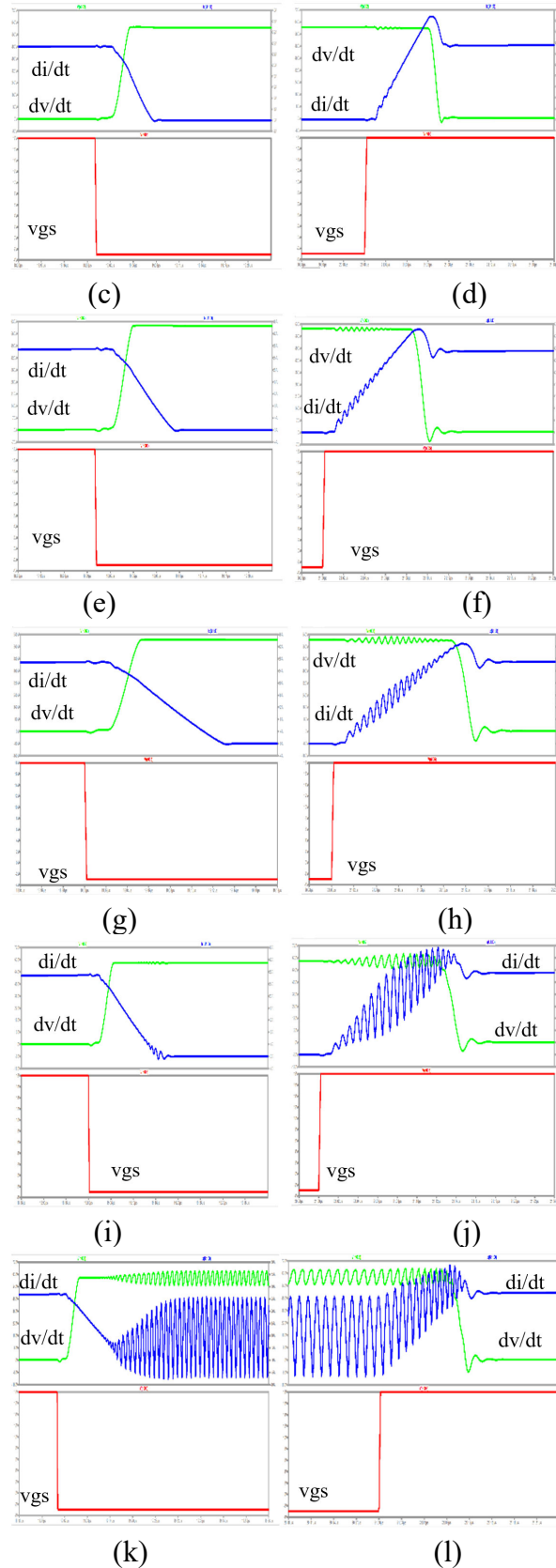


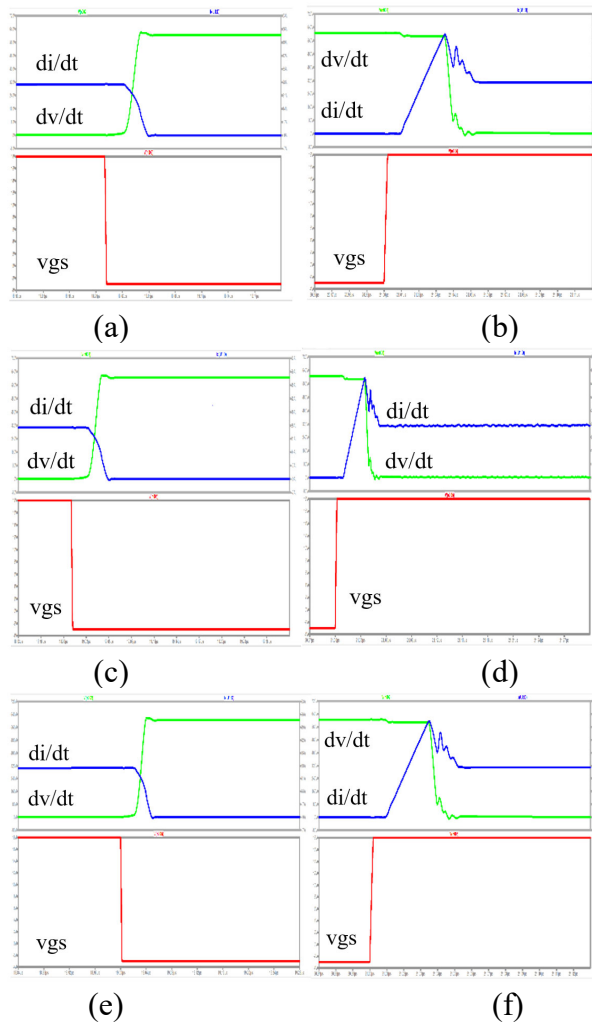
Fig. 7 SiC MOSFETs with different parasitic inductance values are on and off. (a) Turn-off and (b) turn-on with $L_d = L_s=1\text{nH}$, (c) turn-off and (d) turn-on with $L_d = L_s=10\text{nH}$, (e) turn-off and (f) turn-on with $L_d = L_s=20\text{nH}$, (g) turn-off and (h) turn-on with $L_d = L_s=30\text{nH}$, (i) turn-off and (j) turn-on with $L_d = L_s=40\text{nH}$, (k) turn-off and (l) turn-on with $L_d = L_s=50\text{nH}$.

Table 2. SiC MOSFETs switching slew rate with different Ld and Ls

Ld/Ls(nH)	dv/dt(V/ns)		di/dt(A/ns)	
	Turn off	Turn on	Turn off	Turn on
1	31.30	90.41	0.87	1.66
10	28.25	44.31	0.50	0.70
20	24.39	37.45	0.33	0.43
30	20.56	32.99	0.25	0.31
40	20.16	35.26	0.19	0.26
50	17.81	28.14	0.17	0.30

When Ld and Ls equal to 1nH, dv/dt in turn off stage is 31.3V/ns, then the value is the highest, Ld and Ls from 10nH to 50nH in the process of dv/dt has been declining, dv/dt in turn on stage from 1nH to 30nH in the process of DV/DT has been decreasing. It goes up to Ld and Ls equal 40nH, and it goes down to 28.14V/ns when Ld and Ls equal 50nH. di/dt, in the turn off stage, the value has been decreasing with the increase of Ld and Ls; in the turn on stage, when Ld and Ls increase from 1nH to 40nH, di/dt has been decreasing until Ld and Ls reach 50nH, the value does not rise.

Figure 8 tests the effect of parasitic capacitance. The simulation is carried out whenever the value of Cgs is 50pf, 200pF, and 500nF. The simulation occurs whenever the Cgd values are 10pf, 100pf, and 500pf, respectively.



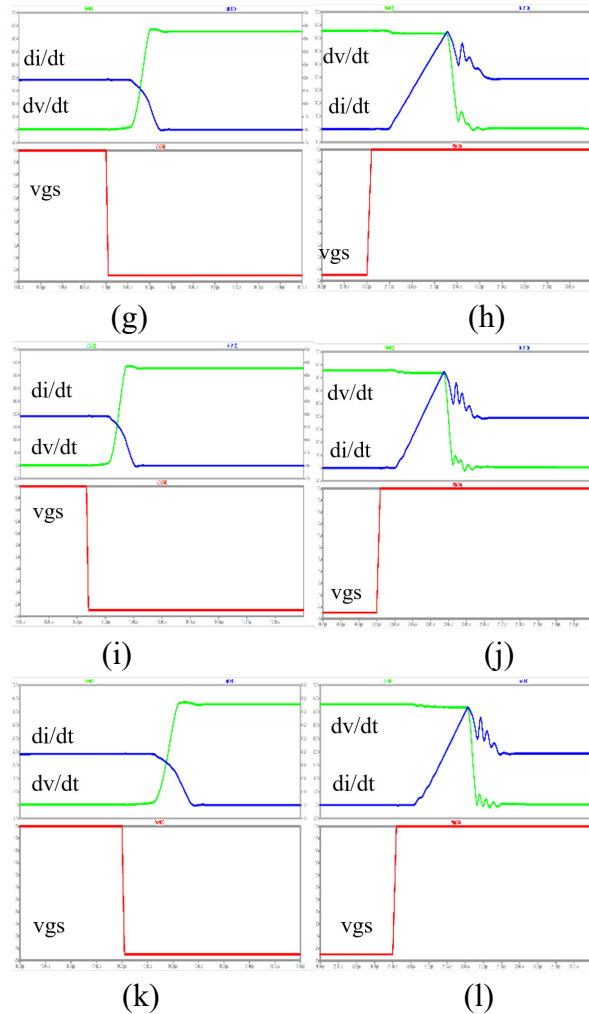


Fig. 8 SiC MOSFETs with Different parasitic capacitors values are on and off. (a) Turn-off and (b) turn-on with $C_{gd} = 10\text{pf}$, (c) turn-off and (d) turn-on with $C_{gd} = 100\text{pf}$, (e) turn-off and (f) turn-on with $C_{gd} = 500\text{pf}$, (g) turn-off and (h) turn-on with $C_{gs} = 50\text{pf}$, (i) turn-off and (j) turn-on with $C_{gs} = 200\text{pf}$, (k) turn-off and (l) turn-on with $C_{gs} = 500\text{pf}$.

4. Conclusion

STspice simulation software was used to build a platform for double pulse testing in this paper, explore the influence of SiC MOSFET gate driver on the switch trajectory, respectively, by adjusting the size of gate resistance, adjust the size of parasitic inductance, adjusting the impact of parasitic capacitance, and then some effects are inevitable, they reduce the performance of SiC MOSFET. Multiple experimental results show how the grid driver affects ringing, overshoot, power loss, switching speed, and other parameters.

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