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Loss evaluation and performance modelling of power electronics for fault management and renewable energy integration

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This work presents the performance and efficiency analysis of solid-state power electronic devices in two complementary applications: fault current limiting and renewable energy integration. A solid-state Fault Current Limiting and Interrupting Device (FCLID) based on a Switched Capacitor (SC) circuit is evaluated for its ability to perform power factor correction and voltage regulation during normal grid operation. Particular focus is given to switching losses in semiconductors, analysed using the PSIM Thermal Module. The 90° phase shift observed between current and voltage in SC circuits is contrasted with in-phase behaviour in DC-DC converters. IGBT losses are calculated and shown to closely align with simulation and literature-based estimates. The second part of the study investigates a grid-connected photovoltaic (PV) system with power smoothing capability, designed to mitigate output fluctuations due to environmental variability. A bidirectional DC-DC converter and a partially controlled lithium-ion battery are used to reduce voltage flicker and improve grid stability. PSIM simulations incorporate MPPT control, inverter modelling, and real-world component characteristics. Losses are primarily concentrated in switching transistors, diodes, and inductors. Across both systems, efficiency is critically evaluated as a primary determinant of performance and economic viability. The simulated and analytical loss results show agreement within 1%, thereby validating the modelling approach. The findings indicate that lower switching frequencies consistently yield overall system efficiencies above 96%, irrespective of whether MOSFETs or IGBTs are employed. However, the study also reveals that reverse recovery losses become negligible compared to conduction losses only at low switching frequencies (<10 kHz) and low current slew rates (di/dt < 100 A/μs). Finally, the analysis demonstrates that practical implementation factors can increase total power losses by up to 21%.

KEYWORDS

solid-state power devices, fault current limiting, power factor correction, voltage regulation, semiconductor losses, PSIM thermal module, grid-connected PV systems, bidirectional DC-DC converter

1 Introduction

The introduction of semiconductor devices in the 1960s revolutionized the power electronics and switched-mode power supply industries (Wilson, 2000; Daryanani, 2024; Rafin et al., 2023). Since then, a wide range of applications has demanded devices with higher efficiency and power density, pushing engineers and researchers to continuously innovate. Material and manufacturing advancements during the 1980s introduced Field Effect Transistors (FETs), which offered lower losses and higher switching frequencies compared to bipolar transistors (Zhang et al., 2025; Bose, , 2009; Rashid, 2011). Continuous innovation also introduced the SiC (Silicon Carbide) and GaN (Gallium Nitride), also known as Wide Bandgap Semiconductors (WBG) which increased the required bandgap energy from 1.1eV offered by the traditional Silicon (Si) to 3.3eV (SiC) and 3.4eV (GaN). These WBG characteristics translated to higher breakdown voltages (i.e. 1,700V) and even lower internal resistances which once again reignited the industry's excitement because of the improved efficiencies (Industry News, 2025; Giovanni Di Maria, 2025; Venus Kohli, 2024; Power Electronic News, 2020). As recent literature reports, WBG based PV grid connected microinverter prototype achieved an efficiency of 96.24% and output voltage THD of 2.51% (Dey et al., 2024) whereas in the case of EV battery charging at a power density of 10.99 kW/L the efficiency was 99.25% (Waheed et al., 2024). Currently, state-of-the-art GaN exhibit internal resistances in the milliohm (mΩ) range and switching frequency capabilities as high as 200 kHz (Xu and Chen, 2017) and even 1 MHz (Lidow et al., 2011) whereas SiC exhibits higher thermal conductivities which is more suitable for high power applications (Davis, 2013; Augustine Fletcher et al., 2025; Bodo's Power Systems Magazine, 2025; Navitas Semiconductors, 2015). A wide range of DC-DC converter topologies including boost, SEPIC, Cuk, and Zeta, designed for applications spanning telecommunications, aerospace, and renewables, are reviewed extensively in (Forouzesh et al., 2017; Jørgensen et al., 2017; Dawidziuk, 2011; Neveu et al., 2014).

Among semiconductor devices dominating switched-mode power supply designs are Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and Insulated Gate Bipolar Transistors (IGBTs) (Bausch, 2011; Mays, 2017; Power Electronics News Magazine, 2020). IGBTs provide higher operating voltages compared to MOSFETs, while MOSFETs offer lower cost and faster switching speeds. This tradeoff is evident in the data tabulated in Tables 1, 2, which have been obtained or derived directly from device datasheets (Ixus, 2021; Mitsubishi, 2013; Infineon, 2024; Infineon, 2001; International Rectifiers). An important criterion for device selection is the characterization of losses, which are broadly classified into conduction and switching losses. For MOSFETs, conduction losses are proportional to the on-resistance ($R_{DS(on)}$) and the drain current (I_D), whereas in IGBTs, conduction losses relate to the collector-emitter saturation voltage ($V_{CE(SAT)}$) and the collector current (I_C) (Sedra and Smith, 2004), (PowerSim Inc, 2017). Switching losses for both devices increase with switching frequency, which directly affects efficiency.

TABLE 1 Igbt characteristics at 25 °C.

Model	I_C (A)	$V_{CE(sat)}$ (V)	Delay (ns)		Rise/ fall (ns)	
			$t_{d(on)}$	$t_{d(off)}$	t_{Rise}	t_{Fall}
IXGT40N60C2D1	75	2.6	18	90	20	32
CM1000HA-24H	1,000	3.6	600	1,200	1,500	350
F3L300R12PT4	460	2.15	210	380	90	70
FF450R12KE4	520	2.15	200	500	45	10
IRGPS60B120KDP	105	2.5	72	366	32	45

Power electronic circuits are commonly simulated using software tools such as Matlab/Simulink, PSpice, LTSpice, PSIM, NI Multisim, TINA Design Suite, *Proteus* Design Suite, SIMPLIS/ SIMetrix, etc (PowerSim Inc, 2017; Electronics Manufacturing Services, 2024; Maithil et al., 2013; Jadhav, 2023; MathWorks, 2005). Each simulation environment represents electronic components and devices using mathematical models, which range from idealized components without parasitic effects to more complex models that include parasitic capacitances, resistances, inductances, and thermal effects. Graphical user interfaces differ: PSpice and PSIM present components as recognizable device shapes, while Matlab/Simulink primarily uses block diagrams, with an additional Simscape Electrical package that offers basic electronic components for connection (MathWorks, 2005).

For performance evaluation, important simulation metrics include simulation time, convergence, memory usage, and overflow stability. Available literature (Debnath et al., 2018; Mohan and Thakura, 2016; Patel et al., 2021; Khader et al., 2010) examining PSIM, Pspice and Matlab/Simulink, agrees on the advantages and disadvantages between the software. PSIM is the easiest to use, generates the fastest results and it is most accurate for system-level power electronics. On the other hand, Pspice uses detailed physics-based device models hence it is widely trusted for component-level validation, and it is excellent for capturing switching transients. Finally, MATLAB/Simulink is the most accurate for control-system and multi-domain integration. On a qualitative level As concluded in (Khader et al., 2010), (Acciani et al., 2006) for complex converter systems such as Voltage Source Converters (VSC), co-simulation between PSIM and Simulink yields the best overall results in these categories. PSIM alone, however, provides the fastest simulation times compared to Simulink and PSpice individually. On a qualitative accuracy basis, the works of (Khader et al., 2010) report the standard deviation on the output simulations; PSIM (σ = 6.422) and Simulink (σ = 12.31). This shows that the results given by PSIM are more clustered, indicating good predictability and repeatability with higher numerical stability and less variation around the mean whereas in the case of Simulink the broader Gaussian spread is better representation of dynamic behavior across the full control range. Hence, Simulink may be considered "better accuracy" if the goal is to capture the entire operating range.

This research employs the PSIM Thermal Module, an add-on to the PSIM program that offers a streamlined method for estimating losses in semiconductor devices (including diodes, IGBTs, and MOSFETs) as well as core and winding losses in inductors (PowerSim Inc, 2017). PSIM component models are categorized

TABLE 2 Mosfet characteristics at 25 °C.

Model	V_{DSBV} (V)	$R_{DS(ON)}$ (mΩ)	I_D (A)	Delay (ns)		Rise/fall (ns)	
				$t_{d(on)}$	$t_{d(off)}$	t_{Rise}	t_{Fall}
STW45NM50	500	70	45	27	22	108	88
SCT30N120	1,200	90	45	19	45	28	20
IRF3805	55	3.3	75	20	87	150	93
GS66516	650	25	60	4.6	14.9	12.4	22

into Ideal, Level 1, and Level 2 models, with Level 2 models including intrinsic and parasitic elements such as gate-to-source, gate-to-drain, and drain-to-source capacitances (C_{gs}, C_{gd}, C_{ds}), which are estimated from datasheet input capacitances (C_{iss}, C_{oss}, and C_{rss}).

The Thermal Module incorporates a device database that not only includes characteristics detailed in manufacturer datasheets but also models the heat transfer path from the transistor junction through the package and case to the heatsink. Users can add new devices and manage the database easily using a provided editor. Devices in the database are then used during simulations to calculate losses using the two main components; the behavioral model and the voltage, current, and temperature data.

The behavioral model of the device, which considers static characteristics such as conduction voltage drop and on-state resistance, but generally excludes dynamic switching transients. For inductors, an ideal inductance model is initially used.

Loss calculations based on voltage, current, and temperature data acquired from the simulation. For switches, PSIM accesses the device database to compute conduction and switching losses, updating static device characteristics for subsequent simulation iterations. For inductors, core and winding losses are calculated based on the device's magnetic material, geometry, winding type, size, and air gap (PowerSim Inc, 2017).

Switching energy losses (E_{on} and E_{off}) are calculated using input parameters such as switching frequency and rise/fall times of voltage and current during transitions. These calculations use voltage and current values immediately before and after switching events. Inductor loss calculations account for material properties and physical construction.

It is important to note that the accuracy of loss calculations depends heavily on the accuracy of the device data. Results should ideally be verified with experimental measurements and adjusted to reflect actual operating conditions.

The goal of this work is to investigate the behavior, performance, and efficiency of semiconductor-based protection and compensation systems for low-voltage distribution networks, with a particular focus on switching losses under both normal and disturbed operating conditions. A secondary aim is to evaluate the integration of a grid-connected photovoltaic (PV) system with energy smoothing capability using a bidirectional DC-DC converter and to quantify system-level losses using PSIM simulation tools. Through comparative analysis and simulation-based validation, this study aims to demonstrate how modern power electronic devices can enhance reliability, power quality, and energy efficiency in distributed energy applications.

The rest of the paper is organized as follows. First, Section 2.0 introduces the protection and correction solid-state device developed for low-voltage distribution networks. Section 2.1 presents the current-voltage characteristics of the semiconductor switches used in the system. Section 2.2 analyzes the losses during normal operation without disturbances, while Section 2.3 focuses on the losses occurring during the compensation period. Section 2.4 provides a discussion on the findings from the previous sections. Section 3.0 shifts focus to the grid-connected PV system with smoothing. Section 3.1 describes the bidirectional DC-DC converter used to interface the battery with the inverter. Section 3.2 covers the design of the low-pass filter, followed by Section 3.3, which introduces the inductor model. Section 3.4 explains the methodology for calculating losses using PSIM, with Section 3.4.1 detailing the transistor investigation and Section 3.4.2 presenting the complete system loss evaluation. Finally, Section 3.5 offers a comprehensive discussion of the results and implications of the PV system analysis.

2 Protection and correction solid state device for low-voltage distribution networks

Low-voltage (LV) distribution networks are the final stage of the electrical grid, delivering power at usable voltages to end-users, typically residential and commercial buildings. To ensure safety and reliability, these networks require protection against over-currents, short circuits, and ground faults which are thoroughly covered under BS7671 IET Wiring Regulations (Institute of Engineering and Technology, 2020) and IEC 61557-1 Electrical safety in low voltage distribution systems (International rectifiers, 2019). In addition, industry practices typically involve placing devices such as current-limiting reactors or fault current limiters (FCLs) in series with the line to restrict and interrupt fault currents (Rafiq, 2018; Shafiul Alam et al., 2018; Dodge, 2024; Gonçalves Sotelo et al., 2022; Office of Electricity Delivery and Energy Reliability, 2012). This series configuration allows the device to directly limit the fault current before it propagates to other parts of the circuit. The use of solid-state breakers/switches in electric power distribution systems has led to advanced technological developments and control methods as extensively reviewed by (Roslan et al., 2024) referencing more than 138 of highly cited works.

The "brilliant" switched capacitor circuit it is mostly used in DC/DC converters, and it is examined by the scientific community

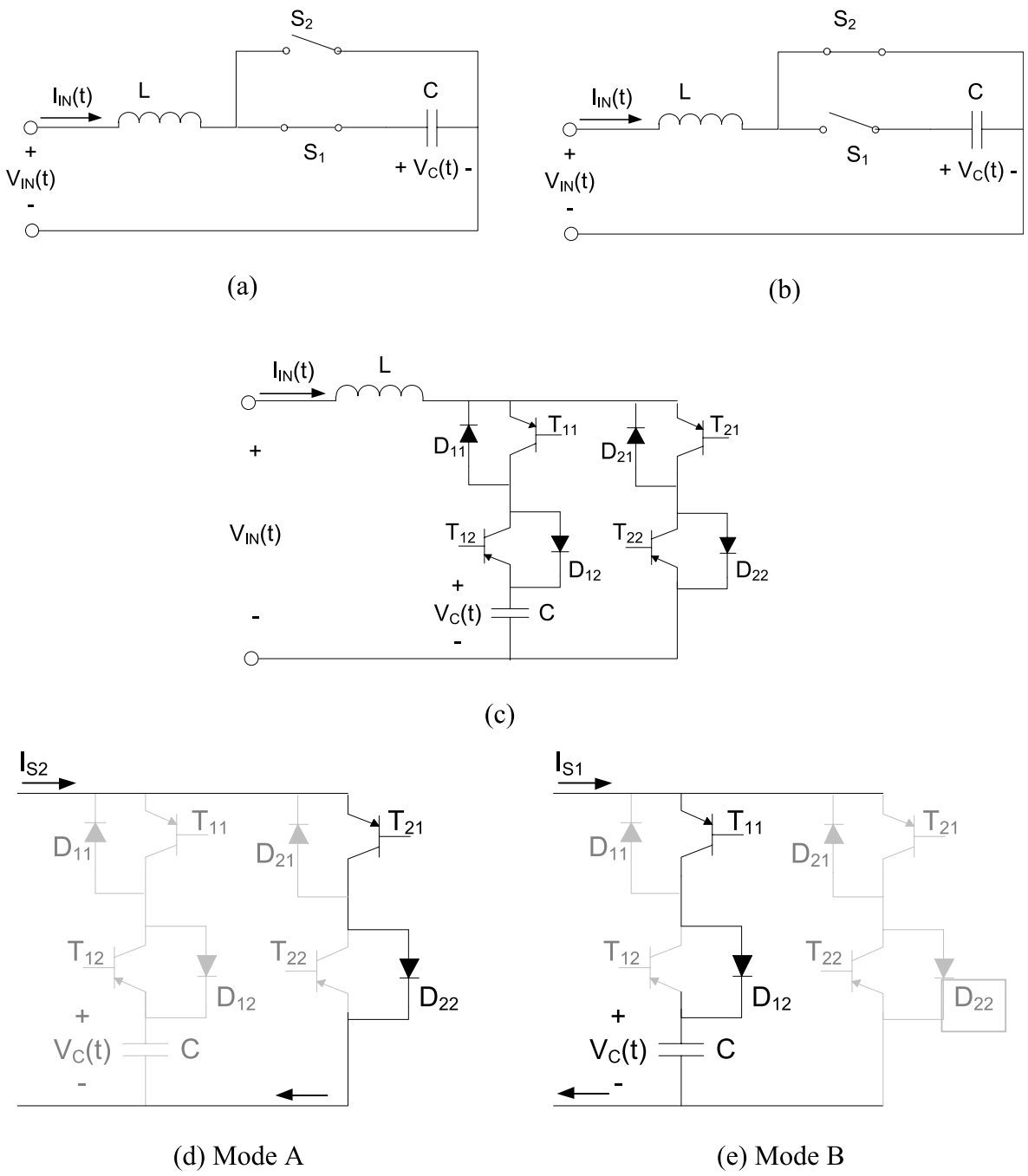

FIGURE 1
(a,b) Modes of the SC circuit **(c)** Implementation of the ideal switch S_1 with bidirectional **(d, e)** Mode A and Mode B of the implemented circuit.

(Sedra and Smith, 2004), (Hertz, 2021; Douglas Seeman, 2006; Gregorian et al., 1983) as well as the industry (Texas Instruments, 2014; Texas Instruments, 2015; Kester et al., 2014; Van Ess, 2000). It precisely controls the flow of energy in a circuit using switches. It is a discrete-time circuit that exploits the charge transfer in and out of a capacitor using switches which are controlled by non-overlapping clocks. The impedance of a switched-capacitor circuit can be changed by adjusting the switching frequency, the capacitance value, or the duty cycle of the switching signals. The use of feedback circuits can modify the effective impedance of the switched-capacitor circuit. In addition, the Generalized Impedance Converter/Circuit (GIC) can make a capacitor mimic some of the characteristics of an inductor (Kumar et al., 2021), (Horio et al., 1985). As shown in Figure 1, when connected in series with the power line it enables fault current control and power quality enhancement (Paterakis et al., 2018; Ahmed et al., 2006; Radmanesh and Gharehpetian, 2015; Radmanesh et al., 2016; Abramovitz and Ma Smedley, 2012; Behzad Naderi et al., 2014; Marouchos et al.,

2006; Marouchos et al., 2014; Marouchos et al., 2017; Ioannou et al., 2007). Under normal operating conditions, it provides power factor correction, while during fault conditions, it effectively limits the fault current to safe levels and facilitates current interruption. A novel contribution of this work is the demonstration of voltage sag correction, where compensation up to 14% is achieved through the careful selection of inductance (L) and capacitance (C) values. The significance of any compensation of 10%–15%, according to BS7671, IEC 61557-1, CBEMA and EN 50549 is that the allowable disconnection time increases from milli-seconds to seconds, hence avoiding nuisance tripping of the available protective devices.

Continuing on a different angle, it is also essential to highlight emerging and innovative applications, such as wireless power transfer. Recent studies have demonstrated that magnetic couplers using an inductor–capacitor–capacitor series (LCC-S) compensation network can deliver a load-independent constant voltage (CV) output in wireless charging systems, making them suitable for integration with distributed energy generation systems like rooftop PV installations. Furthermore, multi-coupling LCC–LCC compensation topologies have been shown to extend the effective charging range of unmanned systems (Wang et al., 2020; Wang et al., 2023; Wang et al., 2025).

However, the insertion of such a circuit into the main power flow of a Low Voltage Distribution Network raises critical questions about its efficiency, particularly because it introduces additional power losses. These losses are predominantly located in the switching semiconductor devices and the transformer, and their accurate estimation is essential for evaluating the device's viability in practical systems.

Unlike typical DC/DC converters, where current and voltage waveforms are generally in phase, the switched capacitor topology introduces a significant phase shift. This work demonstrates that in such circuits, a 90° phase shift exists between current and voltage waveforms. This distinction is crucial, as it impacts the modeling and thermal performance of the switching elements. Therefore, the study pays particular attention to analyzing the phase relationships under a 50 Hz fundamental system frequency and a switching frequency of 5 kHz, as a precursor to modeling and calculating Insulated Gate Bipolar Transistor (IGBT) losses.

2.1 Current-voltage characteristics of the semiconductor switches

To calculate the power losses in the transistors, it is essential to determine both the voltage across and the current through each device. In the switched-capacitor (SC) circuit shown in Figure 1, the duty cycle of switch S_1 is selected such that the current leads the supply voltage. As a result, the capacitor voltage lags the current by 90°. The operating modes of the SC circuit are illustrated in Figures 1a,b. These figures show that the voltage across switch S_1 corresponds to the reversed capacitor voltage, while the voltage across switch S_2 equals the capacitor voltage. The ideal bidirectional switches depicted in Figure 1 are practically implemented using two IGBTs, as shown in Figure 1c.

In the circuit of Figure 1c, current in each branch can flow in both directions. In the capacitor branch, switch S_1 is implemented using two IGBTs, T_{11} and T_{12}, each with its anti-parallel diode (D_{11} and D_{12}). The current through S_1, denoted as I_{S1}, flows in one direction via T_{11} and D_{12}, and in the opposite direction via T_{12} and D_{11}. Similarly, the other branch operates with equivalent behavior.

Figure 2 shows the chopped voltage and current waveforms across the transistors in the circuit of Figure 1a. With S_1 and S_2 implemented using IGBTs, the number of circuit modes increases to four (A, B, C, and D). Only Modes A and B are illustrated in Figures 1d,e, respectively.

In Mode A (Figure 1d), the current is positive and flows downward through T_{21} and D_{22}. The capacitor voltage appears across the non-conducting devices in the opposite branch (T_{11} and T_{12}), with the positive terminal at the collector of T_{12} and the negative at the cathode of D_{11}. Although D_{11} is forward biased, it remains non-conducting, resulting in nearly zero voltage across both D_{11} and T_{11}. Hence, the full capacitor voltage appears across T_{12} in reverse polarity, as seen in Figure 1d. The current waveform is a chopped cosine wave (Figure 1b). Conduction losses in this mode occur in D_{21} and T_{22}.

In Mode B (Figure 1e), the current remains positive, now flowing through T_{11} and D_{12}. The capacitor voltage appears across the non-conducting devices in the other branch (T_{21} and T_{22}), with a positive voltage at the collector of T_{21} and negative at the cathode of D_{22}. As in Mode A, D_{22} is forward biased but non-conducting, so the voltage across D_{22} and T_{21} is negligible. Conduction losses in this mode are in D_{12} and T_{11}.

Switching losses occur during transitions between modes. During the positive current half-cycle, Modes A and B alternate (A → B → A → . . .), while Modes C and D alternate during the negative half-cycle. Each switching frequency cycle includes two mode transitions, such as A → B and back to A (Figure 2).

In each mode transition, one IGBT and one diode turn OFF, while another IGBT and diode turn ON — resulting in two switching events per transition. For instance, transitioning from Mode A to B involves T_{21} and D_{22} turning OFF, and T_{11} and D_{12} turning ON. Since this process happens twice per switching cycle, total switching losses equal four times the loss from a single transistor-diode pair.

At this stage of the study, the reverse-recovery losses in the anti-parallel diodes are assumed to be negligible. This assumption is supported by the manufacturer datasheets (see Table 1), which indicate that the devices are super-fast recovery diodes with recovery times in the nanosecond (ns) range—significantly shorter than those of conventional diodes. Moreover, as suggested in (Bououd et al., 2024), reverse-recovery losses can be further reduced by appropriately controlling the PWM turn-off dead time. Experimental studies such as (Polenov et al., 2009) have also verified that for switching frequencies below 10 kHz, the reverse-recovery losses remain below 0.1 W. Additionally, as demonstrated in (Ioannou et al., 2019a), the application of modulation functions effectively suppresses switching harmonics, which in turn reduces overall system losses. Nonetheless, considering a worst-case scenario, this study will also examine the relationship between the manufacturer-reported losses and the switching frequency, as discussed in Section 4.

More specifically, during the A → B transition:

- T_{21} and D_{22} switch OFF while carrying a current of $I_p\cos(\omega nT)$, and the voltage across them rises to $V_m\sin(\omega nT)$ within t_fall (ns).

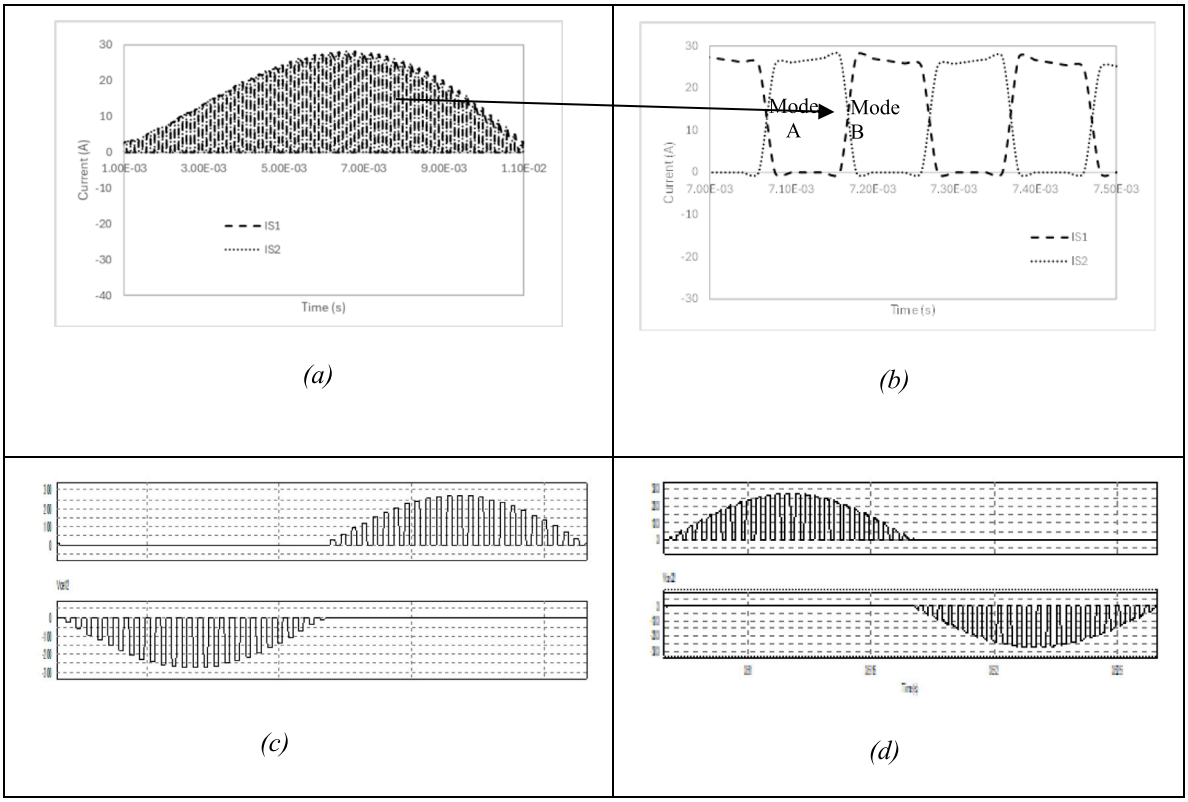

FIGURE 2
(a) Current Through Switches S_1 and S_2. **(c)** Voltage across transistor T11 and T12. **(b)** Mode A during IS1 and Mode B during IS2. **(d)** Voltage across transistor T_{21} and T_{22}.

- Since D_{22} is forward biased in Mode B, its voltage remains negligible, meaning the entire voltage appears across T_{21} (Figure 1E) — even though it is reversed, which poses no issue.
- Simultaneously, T_{11} and D_{12} switch ON, ramping from zero current to $I_p\cos(\omega nT)$, while the voltage across them drops from $V_m\sin(\omega nT)$ to zero within t_rise (ns) (Figure 1C).

Thus, each mode change results in two switching losses: one transistor and one diode turning OFF, and another pair turning ON.

2.2 Losses during normal operation, no disturbance

The application of PSIM's thermal module for analyzing semiconductor device losses was explored in (Ioannou et al., 2019b), while (Paterakis et al., 2018) focused on deriving the theoretical losses of IGBTs. This section examines and compares the PSIM simulation results with the theoretical losses of the IGBT model IXGT40N60C2D1, which is included in the PSIM Thermal Module Database.

As illustrated in Tables 1, 2, state-of-the-art IGBTs can handle significantly higher currents than MOSFETs, but this comes at the cost of much greater switching delays. Therefore, MOSFETs are generally preferred for high-speed switching applications. Figure 3 shows the implementation of a bidirectional switch using two transistors, T_1 and T_2, modeled in the PSIM Thermal Module. This setup replaces switches S_1 and S_2 from Figures 1a,b. The configuration accounts for the thermal resistances of both the transistor and the diode, including the combined thermal resistances from the junction to the case ($R_{th\text{-}jc}$), from the case to the heat sink ($R_{th\text{-}cs}$), and from the heat sink to the ambient environment ($R_{heatsink}$). The ammeters indicate the conduction and switching losses measured in watts.

As shown on Figure 2, the collector current is best described as a half cycle (rectified) sinusoid signal. However, Figure 4 clearly identifies the limits of integration. Hence, the average value given as:

$$I_{C\_AVG} = D\frac{1}{T}\int_{T/2}^{T} I_{C\_peak}\cos(\omega t)dt = D\frac{I_{C\_peak}}{\pi} \tag{1}$$

In addition the saturation collector-emitter voltage V_{CESAT}, is also described as a half cycle (rectified) sinusoid signals with the average value given as:

$$V_{CESAT\_AVG} = D\frac{1}{T}\int_{T/2}^{T} V_{CESAT\_peak}\sin(\omega t)dt \tag{2}$$

$$V_{CESAT\_AVG} = D\frac{V_{CESAT_{peak}}}{\pi} \tag{3}$$

Hence, as shown on Figure 5, the average conduction losses, P_{cond_AVG}, given I_{C_peak} = 33.2A, $V_{CESAT\ \_peak}$ = 1.66V and a switching frequency duty cycle, D of 50%, are given by

$$P_{cond\_AVG} = \frac{I_{C\_peak}V_{CESAT\_peak}}{\pi}D \tag{4}$$

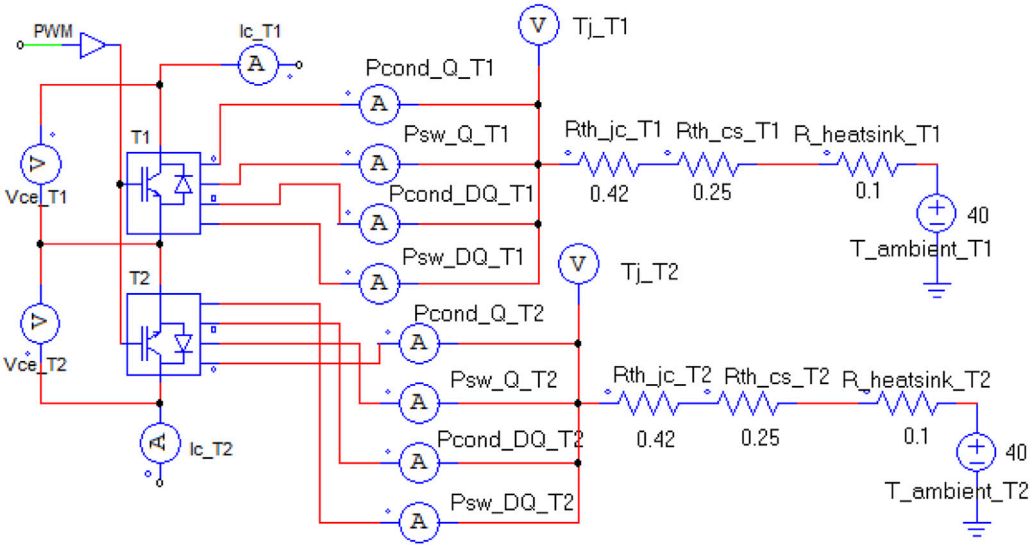

FIGURE 3
IGBT Configuration for conduction in both Cycles.

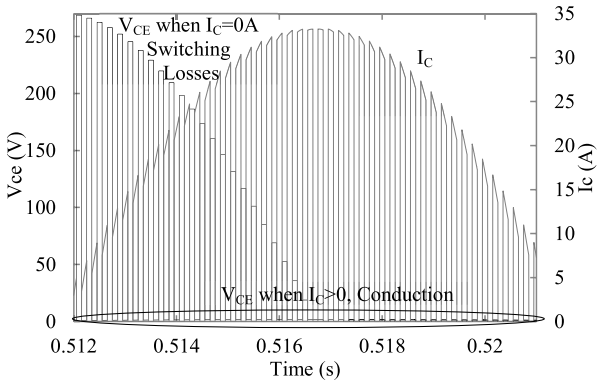

FIGURE 4
IGBT conduction period.

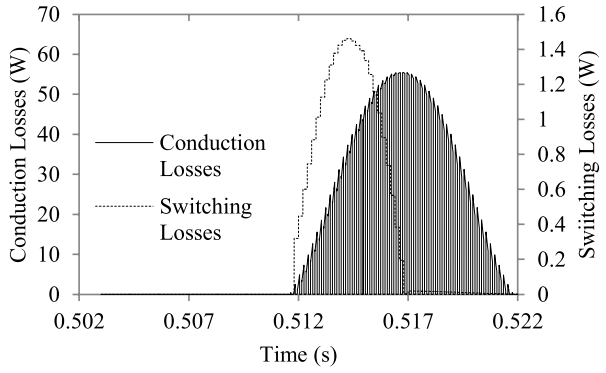

FIGURE 5
IGBT Conduction and Switching Losses for f = 50Hz, f_{SW} = 5 kHz and D = 0.5.

Using (4) the conduction losses are calculated to 8.77W and are also tabulated on Table 3.

Switching losses consist of two main components: turn-on and turn-off losses. These losses account for the time required for current and voltage to transition between the ON and OFF states. As illustrated in Figure 4, these transitions can be represented as rectified quarter-cycle waveforms—one resembling a cosine function and the other a sine function. The average values of these waveforms are given by:

$$V_{CE\_AVG} = D\frac{1}{T}\int_0^{T_4} V_{CE\_peak}\sin(\omega t)dt = D\frac{V_{CE\_peak}}{2\pi} \quad (5)$$

Hence, including the switching delays, V_{CE_peak} is 269V then the losses can be rewritten as:

$$P_{sw} = P_{sw\_ON} + P_{sw\_OFF} \quad (6)$$

TABLE 3 Comparison theoretical (Equations 4, 7) and simulated switching losses.

Theory		PSIM simulation		Difference		% P_{Total}
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	
(W)	(W)	(W)	(W)	(W)	(W)	(%)
8.77	0.213	8.62	0.268	0.15	0.055	1.083

$$P_{sw} = \frac{f_{sw}DI_{C\_peak}V_{CE\_peak}}{2\pi}[t_{RISE} + t_{FALL}] \quad (7)$$

Using Equation 7, the switching losses were calculated to be 0.213 W and are presented in Table 3. It is important to note that the IGBT switching delays were adjusted to account for the rise in

TABLE 4 Comparison summation of dicrete values (Equations 8–10) and simulated switching losses.

Theory		PSIM simulation		Difference		$\%P_{Total}$
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	
(W)	(W)	(W)	(W)	(W)	(W)	(%)
8.77	0.224	8.62	0.268	0.15	0.044	1.18

junction temperature. According to the manufacturer's datasheet, increases in junction temperature do not affect the turn-on delay and rise time; however, the turn-off delay and fall time increase linearly with temperature. For the IXGT40N60C2D1 IGBT, a temperature rise from 25 °C to 46.4 °C results in an increase in turn-off delay (td (off)) from 90 ns to 98.4 ns, and an increase in fall time (t_f) from 32 ns to 40 ns?

Equations 7–10 show the methodology suggested in (Paterakis et al., 2018) where losses are the summation of discrete values. Where V_{CE} and I_C is the peak operating values, T is the period of the switching frequency; M is the number of switching instances in a power cycle. The results are tabulated on Table 4.

$$E_{ON} = \sum_{n=1}^{M_4} \left[t_{RISE} \frac{1}{2} V_{CE} \sin(\omega.T.n) I_C \cos(\omega.T.n) \right] \quad (8)$$

$$E_{OFF} = \sum_{n=1}^{M_4} \left[t_{FALL} \frac{1}{2} V_{CE} \sin(\omega.T.n) I_C \cos(\omega.T.n) \right] \quad (9)$$

For the on-State the lost power is given by

$$P_{LossesSS} = \sum_{n=1}^{M_2} \left[t_{ON} V_{CEON} I_C \sin(\omega.T.n) \right] \quad (10)$$

The total losses using (7) to (9) can be rewritten as:

$$P_{LOSSES} = (P_{OFF} + P_{ON}).f_{sw} + P_{LossesSS} \quad (11)$$

A comparison of the results in Tables 3, 4 reveals that the techniques used—namely, the integration and summation of discrete values—are consistent, with only a minor discrepancy of 0.009 W in the calculated switching losses. An alternative approach, as suggested in (Ioannou et al., 2019b), involves normalizing based on the values provided in the datasheet. However, this method applies exclusively to switching losses. Therefore, Expression (9) can be reformulated as follows:

$$P_{sw} = \frac{f_{sw} D I_C V_{CE}}{2\pi} \left[\frac{E_{ON} + E_{OFF}}{I_C V_{CE}} \right]_{Datasheet} \quad (12)$$

Taken directly from the datasheet for IGBT IXGT40N60C2D1 (Ixus, 2021), I_C = 30A, V_{CE} = 400V, T_j = 25 °C, E_{ON} = 20 mJ and E_{OFF} = 30 mJ then P_{sw} = 0.296W.

A comparison of the results presented in Tables 3–5 indicates that the PSIM simulation yields values that lie between those obtained from the theoretical and normalization methods—effectively representing an average of the two. It is worth noting that a closer review of the PSIM user manual reveals that, for IGBTs, a normalization factor is applied which accounts solely for the effects of the collector-emitter voltage, V_{CE}.

Table 6 presents the total power losses. The multiplication by a factor of four is justified because, within one switching cycle, there are two turn-on and two turn-off events. Specifically, during the half-cycle of positive current—where modes A and B alternate—each mode transition involves switching actions.

Within a single switching cycle, mode A transitions to mode B, and then B returns to A. During each transition, one transistor and one diode switch OFF, while another transistor and diode switch ON. For example, when transitioning from mode A to mode B, transistor T_{21} and diode D_{22} switch OFF, while transistor T_{11} and diode D_{12} switch ON. This process is then reversed when mode B transitions back to mode A.

2.3 Losses analysis for the compensation period

During voltage sags, the system compensates to maintain a nearly constant output load voltage—measured at 331.8 V_{pk} (236.9 V_{RMS}), which represents only a 2.05% deviation from its nominal value prior to the disturbance—as shown in Figure 6. During the compensation period, the duty cycle of the switches (D) is set to 1, meaning that only the branch containing the capacitor is active. Consequently, only two IGBTs—T_{11} and T_{12}, as shown in Figure 1a—conduct during this interval.

As a result, the T_{21} and T_{22} pair remains inactive, contributing zero conduction and switching losses. However, these devices are still subjected to a sinusoidal collector-emitter voltage peaking at 455 V. As shown in Figure 6, a peak voltage of 455 V is observed, corresponding to approximately 33% above the nominal value of 340 V. The duration of this over-voltage is clearly less than half a cycle, i.e., below 10 ms. This raises the question of whether such a transient is acceptable. According to the industry standards defined by CBEMA, over-voltages in the range of 140%–150% of nominal voltage are permissible for durations up to 10 ms. Furthermore, EN 50549, which specifies voltage disconnection time limits, considers over-voltage events significant only when their duration exceeds 10 cycles (200 ms)—a period much longer than that observed in this study. Therefore, it can be concluded that the proposed compensation method is compliant with both CBEMA and EN 50549 standards, effectively preventing nuisance tripping of protective devices.

During compensation the conducting pair of IGBT is kept ON with a duty cycle of 100%, D = 1. The collector current, I_C is 32.4A and the collectro-emitter voltage, V_{CE} is 1.65V. The simulated junction temperature is 52 °C. Figure 7 show the simulated IGBT conduction losses. Hence, since the conductions losses of Figure 7 looks like a half wave rectified sinusoid then the methodology described using Equations 1–7 was used. The theoretical results are tabulated on Table 7. The values are for a single IGBT.

2.4 Discussion

A Fault Current Limiter is presented in which a Switched Capacitor (SC) circuit is utilized both for power factor (P.F.) correction and as a solid-state Fault Current Limiting and Interrupting Device (FCLID) suitable for low-voltage distribution

TABLE 5 Comparison datasheet normalisation (Equation 12) and simulated switching losses.

Datasheet normalization	PSIM simulation	Difference	%Difference
P_{sw}	P_{sw}	P_{sw}	
(W)	(W)	(W)	(%)
0.296	0.268	0.028	9.46

TABLE 6 Total power losses for the 4 IGBT.

Datasheet normalization	PSIM simulation	Theory	%Difference
$P_{cond} + P_{sw}$	$P_{cond} + P_{sw}$	$P_{cond} + P_{sw}$	
(W)	(W)	(W)	(%)
4x (0.296 + 8.77)	4x (8.62 + 0.268)	4x (8.77 + 0.213)	1.06
4 × 9.066	4 × 8.888	4 × 8.983	
36.264	35.552	35.932	

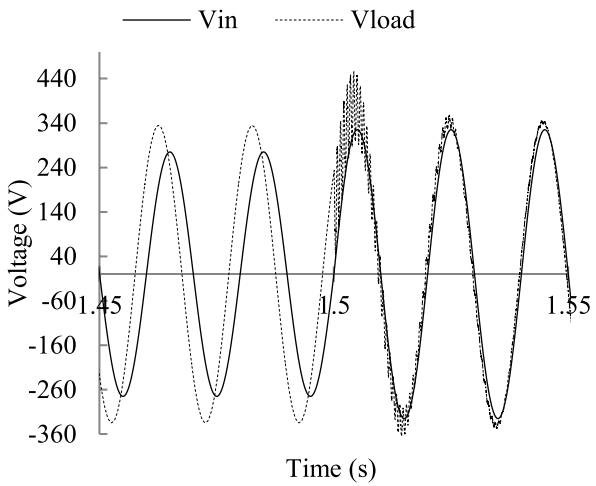

FIGURE 6
System compensates for voltage sag.

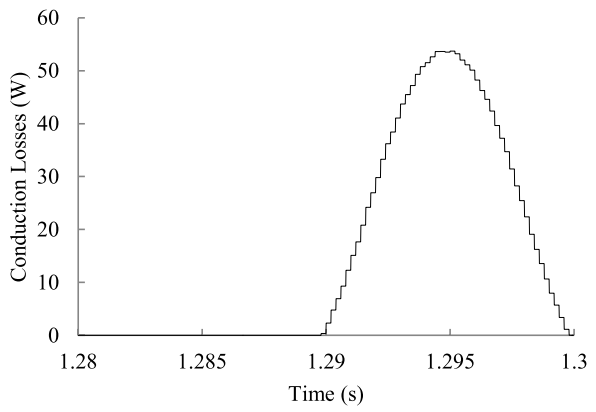

FIGURE 7
Conduction losses.

TABLE 7 Comparison theoretical and simulated switching losses.

Theory		PSIM simulation		Difference		$\%P_{total}$
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	
(W)	(W)	(W)	(W)	(W)	(W)	(%)
17.03	6.6u	15.6	5.7u	1.43	0.9u	8.4

networks. Control is achieved by adjusting the duty cycle of the switching devices, with the selection of the inductance (L) and capacitance (C) values playing a critical role. Optimization is applied to achieve a power factor correction to a target value of 0.85 while maintaining the load voltage within acceptable limits. For a lagging power factor of 0.85, the load voltage is consistently 5% higher than the supply voltage.

A key innovation of this work is the introduction of sag voltage correction, leveraging the inherent voltage boost provided by the SC circuit. As demonstrated, a balance is achieved between power factor improvement and a tolerable increase in load voltage—enhancing the power factor to 0.85 while limiting the voltage increase to only 5%. Furthermore, it is shown that the load voltage can be elevated by up to 12.5% relative to the nominal voltage at the point of connection. This is particularly beneficial during voltage sag events; for instance, a voltage sag of 15.3% is corrected back to 236.9 V_{RMS} (331.8 V_{pk}), representing only a 2.05% deviation from the pre-disturbance value. The significance of any compensation of 10%–15%, according to BS7671, IEC 61557-1, CBEMA and EN

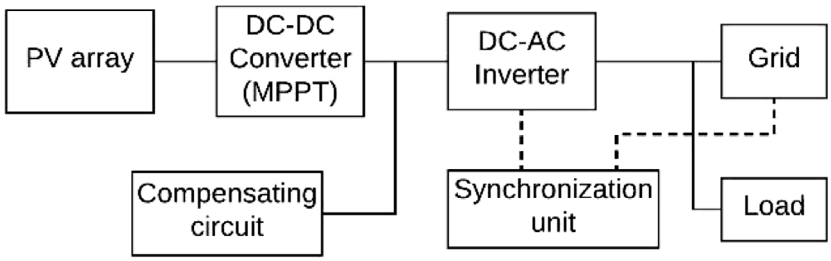

FIGURE 8
The PV system supplying the load and the grid with compensation circuit (Augustine Fletcher et al., 2025)

50549 is that the allowable disconnection time increases from milliseconds to seconds, hence avoiding nuisance tripping of the available protective devices.

Switching semiconductor losses are analysed using the PSIM Thermal Module. It is shown that in switched capacitor circuits, there is a 90° phase shift between current and voltage. A comparison between theoretical and simulated losses reveals a difference of 150 mW in conduction losses and 30 mW in switching losses.

Finally, because this process is repeated once every switching cycle, the total switching losses per cycle amount to four times the losses of a single transistor, resulting in a total power dissipation of 42 W.

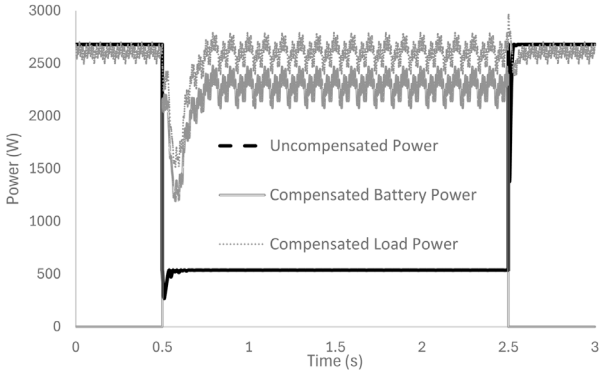

FIGURE 9
Uncompensated and compensated load power.

3 The grid connected PV system with smoothing

The photovoltaic (PV) array converts solar energy into electrical power. For a given level of solar irradiance, there exists a unique Maximum Power Point (MPP), defined by the corresponding voltage (V_{mpp}) and current (I_{mpp}). The Maximum Power Point Tracker (MPPT), typically implemented using a DC-DC converter, is responsible for adjusting the operating point of the PV array to match the DC input voltage level of the inverter. This ensures that the PV modules operate at their maximum power output. The inverter then converts the DC voltage into a 50 Hz AC voltage synchronized with the grid.

The MPPT is controlled via the duty cycle (D) of its switching transistor. In the inverter, two control parameters are used: the modulation index (D_m) and the phase angle (δ). The modulation index determines the output voltage magnitude, while δ controls the phase angle between the inverter output and the grid voltage—thus regulating the amount of power transferred to the grid.

Solar irradiance incident on the PV modules fluctuates due to variable cloud coverage, which is inherently unpredictable. Sudden reductions in irradiance, such as when clouds obscure the sun, lead to corresponding drops in power generation. These power fluctuations propagate through the system, ultimately affecting the output power delivered to the grid (Thekaekara, 1976). Such variations can lead to power quality issues and may compromise grid stability (Parra et al., 2014), (Argyrou et al., 2018).

A promising solution involves the integration of short-term energy storage systems to mitigate these fluctuations and enhance overall system performance (Beaudin et al., 2010; Senjyu et al., 2008; Seo et al., 2010; Wang et al., 2018). In this work, a lithium-ion battery is connected to the 400 V DC bus at the inverter input via a bidirectional DC-DC converter, as illustrated in Figure 8.

The impact of solar irradiance disturbances on PV modules due to cloud movement is simulated in PSIM by introducing a sudden drop in irradiance from 1000 W/m^2 to 200 W/m^2 for a duration of approximately 2 seconds, as shown in Figure 2. This drop in irradiance significantly affects the output current of the PV system. Prior to the disturbance, the current at the inverter input is 6.415 A (Figure 9), which drops to 1.185 A during the irradiance reduction. Consequently, the compensating circuit supplies the difference—approximately 5.23 A—during the disturbance period.

Under normal conditions (without disturbance), the system delivers 2.566 kW of power to the grid. When the irradiance drops, the PV array contributes only 473.9 W, while the compensating circuit provides an additional 2.092 kW. This ensures continuity and stability in power delivery to the grid. The additional energy is drawn from a lithium-ion battery, which serves as the short-term energy storage element.

As illustrated in Figure 9, the implementation of the compensating circuit markedly improves the system's dynamic performance. After a brief transient period of approximately 180 ms, both the inverter input current and the power delivered to the grid recover to values close to their original steady-state conditions. According to CBEMA standards, undervoltage transients down to 70% of the nominal voltage are permissible

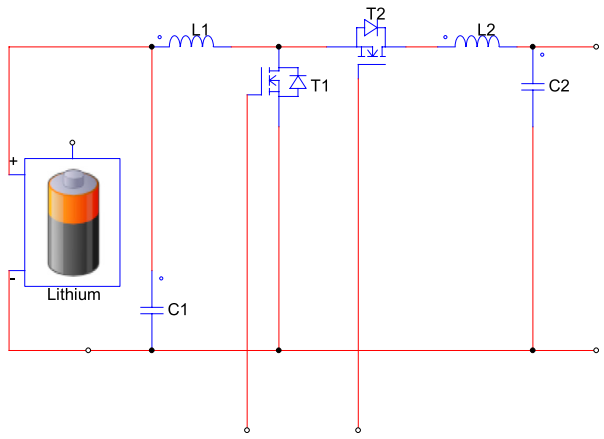

FIGURE 10
The bidirectional DC to DC converter.

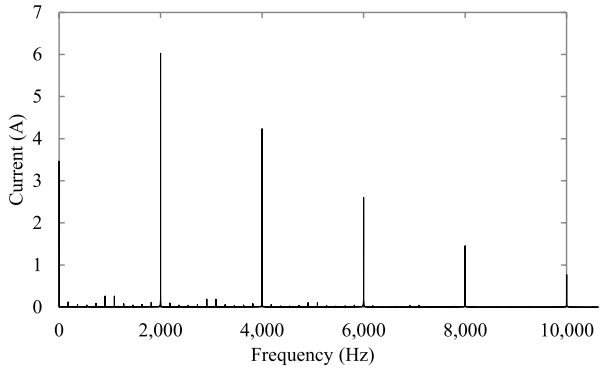

FIGURE 11
Fourier fast transform (FFT) for the load current without filtering.

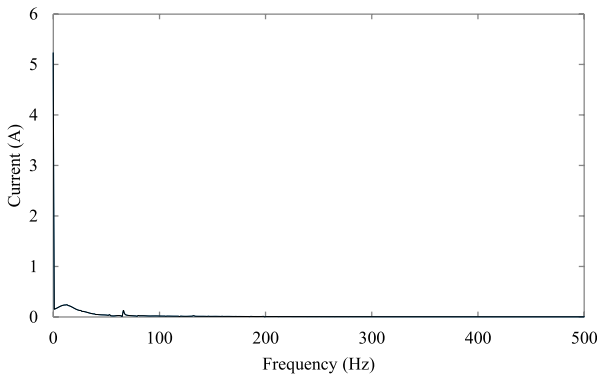

FIGURE 12
Fourier fast transform (FFT) for the load current including filtering.

for durations up to 200 ms. Therefore, the battery-compensated system, which restores full load power within 180 ms, demonstrates compliance with these standards and effectively prevents nuisance tripping of protective devices.

3.1 The bidirectional DC to DC converter

The main sources of losses of the bidirectional DC-DC converter shown in Figure 10 are the transistor, the diode and the two inductors L_1 and L_2. The output low pass filter L_2 and C_2 is designed to minimise the output ripple of the current.

3.2 Design of the low pass filter

Figure 11 illustrates that, without any filtering, switching frequency harmonics are present, resulting in a distorted current waveform. To determine the appropriate value for the smoothing capacitor, the approximation method outlined in (Marouchos et al., 2014) and (Marouchos et al., 2017) is employed.

$$C = \frac{I_{pk}}{4 f V_{ripple}} \tag{13}$$

Any LC circuit can be described by a second-order differential equation. Second-order filters provide an attenuation slope of 40 dB per decade. Specifically, a single-stage LC low-pass filter achieves this 40 dB/decade attenuation, while a two-stage LC filter doubles the slope to 80 dB/decade. However, single-stage filters tend to exhibit fewer resonance issues compared to two-stage configurations. Additionally, LC filters are generally more efficient, with lower losses, than filters that incorporate resistors for damping purposes (Kunzi and Bailey, 2015), (Zhang, 2017). For the present design, a single-stage LC filter was selected, with its resonant frequency defined as:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{14}$$

As clearly demonstrated by the Fast Fourier Transform (FFT) in Figure 12, the harmonics have been effectively attenuated by the single-stage LC low-pass filter with L = 18.1 μH and C = 35,000 μF. The approximation technique successfully met the design objectives. It is worth noting that increasing the capacitance value reduces the load current ripple but also leads to a longer rise time and an increased duration to reach steady-state equilibrium.

3.3 Inductor model

The inductor thermal model in PSIM currently does not allow the direct setting of the ohmic DC resistance (DCR). For a given inductance, it assumes an excessively high DCR value, resulting in unrealistically large copper losses (P_{wind}), as shown in Table 11. Moreover, Table 11 indicates that the predicted winding losses alone exceed the total system losses, signaling the need for further investigation. A detailed review of the PSIM user guide (PowerSim Inc, 2017) recommends verifying inductor losses through experimental measurements and applying calibration factors to the simulation results. This limitation may explain why manufacturers provide online tools that assist engineers in

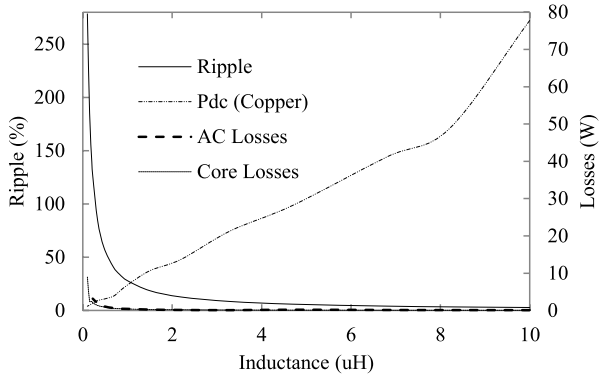

FIGURE 13
Inductance versus ripple and losses.

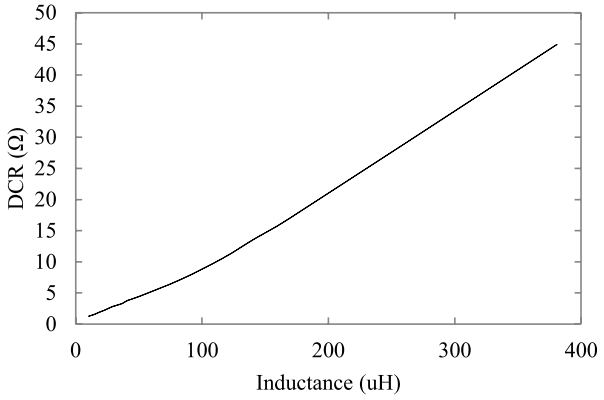

FIGURE 14
Inductance *versus* DCR.

calculating core and winding losses for various converter topologies (Vishay, 2015; West Coast Magnetics, 2016; CoilCraft, 2017).

The data presented in Figure 13 is either obtained directly or derived from sources (Ioannou et al., 2007; Wang et al., 2020; Wang et al., 2023) for a converter operating with a load current between 26 and 35 A. The magnetic flux density, B, was obtained or derived directly from the manufacturers' datasheet, at 8655 G (8.655×10^{-3} T) for an inductance of 0.1 μH and 347.5 G (3.475×10^{-4} T) for 10 μH. Figure 13 illustrates that as the inductance of the inductor increases, copper losses (I^2R) become the dominant source of energy loss, while both ripple current and losses (AC and core) decrease exponentially. The inductor's DC resistance (DCR) significantly influences the ripple current and copper losses. Higher inductance values correspond to increased DCR, which limits peak current, reduces the time constant, raises the damping factor, and consequently suppresses oscillations and current ripple.

Figure 14 illustrates the relationship between inductance and DC resistance for commercially available, state-of-the-art, low-loss, high-current inductors. The DC resistance (DCR) is expressed by the following quadratic equation:

$$DCR = 0.0001L^2 + 0.00791L + 0.3312 \quad (15)$$

where DCR is measured in milliohms (mΩ) and L is the inductance in microhenries (μH). Based on this equation, a 1,000 μH inductor would have an extrapolated DC resistance of approximately 79.5 mΩ.

3.4 Calculation of losses using PSIM

The bidirectional DC-DC converter is used as a benchmark to evaluate the application of PSIM for loss calculation, as illustrated in Figure 8. Initially, the losses in the bidirectional converter are determined through PSIM simulation, after which the same technique is applied to the complete grid-connected system. Figure 8 depicts the circuit employing switching components from the thermal database. These components feature additional terminals that facilitate the calculation of both conduction and switching losses.

It is worth noting from Figure 15 that the semiconductor switching devices account for the thermal resistances of both the transistor and the diode, including the combined thermal resistances from the junction to the case ($R_{th\text{-}jc}$), the case to the heat sink ($R_{th\text{-}cs}$), and the heat sink to the ambient ($R_{heatsink}$).

3.4.1 Transistor investigation

Four MOSFETs were compared in this study. The characteristics listed in Table 1 were either directly obtained from or derived based on the device datasheets (STMicroelectronics, 2018; STMicroelectronics, 2019; International Rectifier, 2020; GaN Systems, 2021). All selected devices are included in the PSIM thermal module database. For the simulations, MOSFET switching was implemented using a standard Pulse Width Modulation (PWM) technique with a triangular wave and comparator (Choudhary et al., 2012), (Ranjan et al., 2017).

It is worth noting from Table 8 that the drain-source voltage (V_{DS}) is defined as the voltage at which no more than the specified drain current flows at a given temperature (25 °C) with zero gate-source voltage (V_{GS} = 0). This corresponds closely to the actual avalanche breakdown voltage (Sedra and Smith, 2004). For this design, when V_{GS} = 0, the average V_{DS} is 77 V, the drain current (I_{DS}) is 24 A, and the junction temperature for the IRF3805 reaches approximately 230 °C. The elevated temperature introduces a normalized factor that increases the drain-to-source voltage by 40%–50%. Therefore, under these design conditions, the avalanche breakdown voltage is never reached.

All load currents listed in Tables 9, 10, after smoothing, exhibit a current ripple of less than 1 A peak-to-peak. The efficiency, η, shown in the tables is defined as the ratio of output power to input power, where the output power is the load power ($I_{av} \times V_{av}$) and the input power is the battery power ($I_{av} \times V_{av}$). Note that the battery voltage is 78.5 V while the load voltage is 400 V. The results indicate that at a switching frequency of 2 kHz, the MOSFET with the lowest $R_{DS(on)}$ achieves the highest efficiency of 95.85%.

It is worth noting that the load currents listed in Tables 9, 10 vary by approximately 10% between their minimum and maximum values. This variation is attributed to the $R_{DS(on)}$ of the MOSFETs. When $R_{DS(on)}$ is at its lowest (3.3 mΩ), the battery

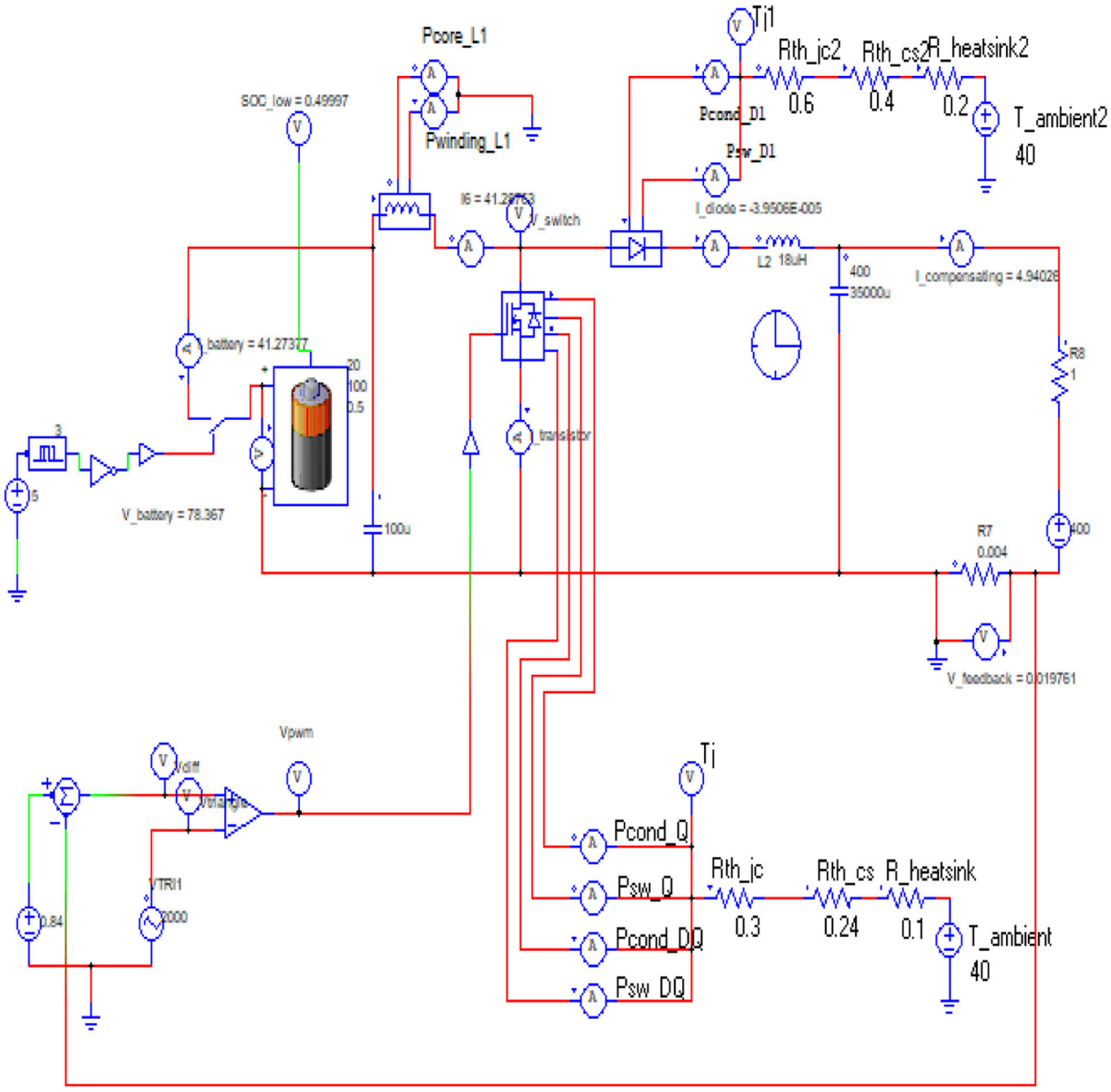

FIGURE 15
Simulation of the bidirectional converter using the PSIM Thermal model.

current—and consequently the compensating current—is the highest. Conversely, when $R_{DS(on)}$ is at its highest (90 mΩ), the battery current decreases, leading to a lower compensating current.

In Table 11 the individual losses of each component are displayed. Total System losses are the difference of input-output power derived from the data in Table 9. The copper losses of the inductor as noted above are excessively high. On the other hand, as can be seen, the inductor winding losses alone exceed the systems total losses. As explained above the ohmic resistance DCR of the inductor is derived from expression (15).

Circuit theory identifies the primary losses in the system as occurring in the semiconductor switching devices (MOSFETs and diodes) and the inductor (Electronics Manufacturing Services, 2024). Semiconductor devices exhibit two types of losses: conduction and switching. Conduction losses are mainly resistive (I^2R) due to the MOSFET's $R_{DS(on)}$, while switching losses account for the energy dissipated during turn-on and turn-off transitions. Inductors experience two types of losses as well: core losses and winding losses. Core losses arise from the magnetic properties of the core, including hysteresis and eddy currents, whereas winding losses consist of resistive (copper) losses and AC losses caused by skin and proximity effects. Both types of losses are evaluated using the PSIM Thermal Module (Bodo's Power Systems Magazine, 2025).

The ohmic resistance of the inductor DCR is calculated from expression (3) and the results for component losses are shown in Tables 12, 13 at two different switching frequencies.

TABLE 8 Mosfet characteristics.

Model	Type	V_{DSBV} (V)	$R_{DS(ON)}$ (mΩ)	I_D (A)	$R_{Thermal}$ (Ω)		Rise/fall (ns)	
					jc	*cs*	t_{Rise}	t_{Fall}
STW45NM50	SiC	500	70	45	0.3	0.24	108	88
SCT30N120	SiC	1,200	90	45	0.65	0.24	20	28
IRF3805	SiC	55	3.3	75	0.45	0.24	150	93
GS66516	GaN	650	25	60	0.27	0.24	12.4	22

*V_{DSBV} - Drain-to-Source Breakdown Voltage.

TABLE 9 System efficiency results: switching frequency, Fsw = 2 k_{Hz}.

Model	Battery			Load		Efficiency
	V_{av}	I_{av}	P_{av}	I_{av}	P_{av}	
	(V)	(A)	(W)	(A)	(W)	(%)
STW45NM50	78.5	28.3	2218	4.97	2013	90.74
SCT30N120	78.5	28.4	2231	5.1	2066	92.60
IRF3805	78.5	29.7	2331	5.51	2234	95.85
GS66516	78.5	28.8	2260	5.28	2140	94.68

TABLE 10 System efficiency results: switching frequency, Fsw = 8 kHz.

Model	Battery			Load		Efficiency
	V_{av}	I_{av}	P_{av}	I_{av}	P_{av}	
	(V)	(A)	(W)	(A)	(W)	(%)
STW45NM50	78.6	29.1	2282	4.86	1968	86.22
SCT30N120	78.5	28.7	2449	4.93	1996	81.52
IRF3805	78.5	28.7	2252	5.1	2066	91.74
GS66516	78.5	28.6	2245	5	2025	90.20

The component losses listed in Tables 12, 13 show that the MOSFET with the lowest $R_{DS(on)}$ has the lowest conduction losses (P_{cond}). Additionally, switching losses increase with switching frequency; doubling the switching frequency (f_{sw}) results in approximately doubling the switching losses (P_{sw}). However, the MOSFET IRF3805 exhibits the lowest conduction losses but the highest switching losses. This is due to its rise and fall times (t_r = 150 ns and t_f = 93 ns), which are significantly longer than those of the other MOSFETs, whose rise and fall times are around 35 ns and 23 ns, respectively, as stated in the datasheets.

3.4.2 Calculation of losses using PSIM of the complete PV system

The described methodology is applied to two scenarios. Scenario one simulates the standalone PV grid-connected system, while Scenario two simulates the PV system integrated with the compensating circuit.

Simulation results in Tables 14, 15 for Scenario one indicate a system efficiency of 95.3%. The PV system generates 2,658 W, with 2,558 W delivered to the grid—values measured directly from the circuit. The losses, calculated as the difference, amount to 127 W. Applying the described methodology, including the inductor's DCR and summing all individual losses, yields total system losses of 135 W. This results in a 5% error and a slight efficiency reduction to 95%.

For Scenario 2 (Tables 16, 17), the PV array generates 539 W, with the battery contributing an additional 2,449 W. The total power

TABLE 11 Comparison between system total losses and psim simulated losses; Fsw = 2 kHz.

Model	System total Losses	PSIM simulated component losses					
		Inductor		Diode		MOSFET	
		P_{core}	P_{wind}	P_{cond}	P_{sw}	P_{cond}	P_{sw}
	(W)	(W)	(W)	(W)	(W)	(W)	(W)
STW45NM50	205	2.2	1,347	1.6	1.3	126	1.1
SCT30N120	165	2.3	1,587	7.2	1.6	77	1.3
IRF3805	97	2.4	2160	8	1.7	2.6	16.5
GS66516	120	2.4	1,686	7.5	1.7	34	0.2

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TABLE 12 Losses of individual components and calculated inductor winding; Fsw = 2 kHz.

Model	PSIM simulated component losses					
	Inductor	Inductor	Diode		MOSFET	
	P_{copper}	$P_{core+AC}$	P_{cond}	P_{sw}	P_{cond}	P_{sw}
	(W)	(W)	(W)	(W)	(W)	(W)
STW45NM50	64	2.2	1.6	1.3	126	1.1
SCT30N120	64	2.3	7.2	1.6	77	1.3
IRF3805	70	2.4	8	1.7	2.6	16.5
GS66516	66	2.4	7.5	1.7	34	0.2

fed to the grid is 2,814 W, corresponding to a system efficiency of 94.2% and losses of 174 W. Using the same loss calculation approach, total losses are estimated at 183 W, resulting in a 4% error and a marginal efficiency decrease to 93.9%.

For both scenarios, the inverter power was the same as shown on Table 15 because the generated power remained stable at 2.5 kW even during the disturbance conditions.

3.5 Discussion

The losses of a grid connected system with smoothing are derived by employing PSIM. It is demonstrated that PSIM has the tools for this task. Commercially available transistors and diodes can be modelled with their characteristics considered including the heatsink. Inductors models in PSIM require calibration factors using experimental data.

Analysis of the losses of individual components has shown that for the low switching frequencies employed, the losses are small and follow as expected almost linearly the switching frequency. Therefore, switching losses can be extrapolated for higher switching frequencies.

In the case of Inductors, the analysis of the individual losses show that at higher inductance values the winding losses are much higher than the core and AC losses. The winding losses also known as copper losses are given by i^2R, where R is the DC resistance of the winding. Specialized, state of the art, low loss and high current inductors offer very low DCR.

4 Experimental results

The results obtained thus far indicate that the PSIM Thermal Module aligns closely with theoretical calculations, exhibiting an accuracy within 1%–2%. This level of agreement is expected, as the thermal module enables the user to input component parameters extracted or derived directly from manufacturer datasheets. However, in light of recent studies concerning reverse-recovery losses, this section aims to examine relevant experimental data in greater detail.

The first parameter investigated is the $R_{DS(on)}$ resistance. In this work, $R_{DS(on)}$ was initially assumed constant, with datasheet values applied throughout the analysis. As shown in Figure 16, for the MOSFET IRF3805, $R_{DS(on)}$ decreases significantly falling below 10 mΩ when V_{GS} ranges between 15 and 20 V. Despite this, a constant resistance of 3.3 mΩ was assumed in the simulations. As illustrated in Figure 17, this simplification introduces an error between 5% and 27%, with an average deviation of approximately 18%. This discrepancy directly impacts the conduction loss estimation, which increases proportionally. The subsequent analysis therefore extends the comparison to include the contribution of reverse-recovery losses.

By analyzing the drain–source switching voltage and current waveforms shown in Figure 18, the switching parameters were determined as follows: t_{on} = 204 ns, t_{off} = 260 ns, and a current rate of change of di/dt = 49 A/μs. These values were then compared with the corresponding datasheet specifications of 170 ns, 180 ns, and 100 A/μs, respectively. It is important to note that the measured turn-on and turn-off durations do not represent the reverse-recovery time, which is a distinct and critical parameter when calculating reverse-recovery losses, as shown in the following equations.

$$Q_{rr} = \frac{1}{2} I_F t_{rr} \tag{16}$$

$$E_{rr} = Q_{rr} V_r \tag{17}$$

$$P_{rr} = E_{rr} f_{SW} \tag{18}$$

Where subscript *rr* is for *reverse recovery*. Then Qrr is the reverse recovery charge in (nC), I_F is the forward current in (A), t_{rr} is the

TABLE 13 Losses of individual components and calculated inductor winding; Fsw = 8 kHz.

Model	Inductor	PSIM simulated component losses				
	Calculation	Inductor	Diode		MOSFET	
	P_{wind} I^2DCR	$P_{core+AC}$	P_{cond}	P_{sw}	P_{cond}	P_{sw}
	(W)	(W)	(W)	(W)	(W)	(W)
STW45NM50	67	0.3	6.9	7.3	129	4.6
SCT30N120	65	0.3	7	7.2	72.7	5.4
IRF3805	65	0.3	7.3	7.3	3	64
GS66516	65	0.3	7.1	7.2	28.9	0.8

10.3389/felec.2025.1675666

TABLE 14 Scenario 1 losses in MPPT.

MPPT PV boost converter P_{Loss} = 40.49W							
MOSFET				Diode		Inductor	
Diode		MOSFET					
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{core}	P_{wind}
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
0	0	0.42	8.8	9.4	0.7	1.2	19.97

TABLE 15 Scenario 1 losses in inverter.

Inverter losses 93.5W			
Diodes		MOSFETs	
P_{cond}	P_{sw}	P_{cond}	P_{sw}
(W)	(W)	(W)	(W)
4.02	0	67	20.8

TABLE 16 Scenario 2 losses in MPPT.

PV boost converter P_{Loss} = 5.08W							
MOSFET				Diode		Inductor	
Diode		MOSFET					
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{core}	P_{wind}
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
0	0	0.28	2.2	1.2	0.1	0.5	0.98

time in ns, E_{rr} is the energy in n*J*, f_{sw} is the switching frequency in (*Hz*) and finally Prr is the power in (W).

As shown in Figure 19, the current rate of change (dt/dt) is a very important parameter because the higher the rate results in higher reverse recovery losses. As clearly shown by increasing the rate from 100 to 800 A/us the Qrr increases by a factor of 4.

With the new information at hand then the additional results for the Switched Capacitor and complete PV system applications are tabulated on Tables 18–21. The comparison includes the simulated/theoretical results and the scenarios with practical considerations yielding from literature and experimental processes.

As can be seen from Tables 18–21, for the switched capacitor application the inclusion of practical considerations has increased the power losses by 20.45%. This shows transistor internal resistances cannot be considered as constant and the Reverse Recovery losses cannot be ignored without investigation. In the case of PV grid connected system, the practical consideration increased the total system losses by 5.6%.

TABLE 17 Scenario 2 losses in bidirectional converter.

Battery boost converter P_{Loss} = 85W							
MOSFET				Diode		Inductor	
Diode		MOSFET					
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{core}	P_{wind}
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)
0	0	2.6	16.5	8	1.7	1.2	55

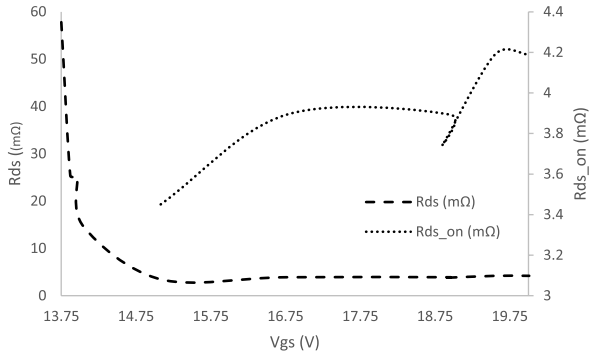

FIGURE 16
R_{DS} (on) resistance of MOSFET IRF3805.

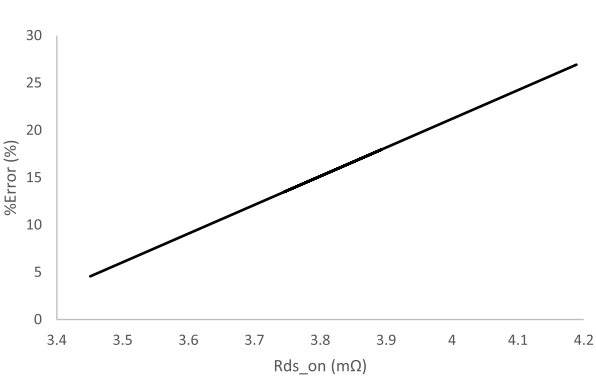

FIGURE 17
R_{DS} (on) %error.

Worth noting that the losses of the bidirectional converter and the MPPT subsystems only increased by less than 3% whereas the Inverter alone increased by 11.31%. This is reasonable considering that direct effect on the operating currents and voltages. However, it is very important to note that the switching frequency can significantly affect the losses. For both applications the switching frequencies were 5 and 2 kHz respectively. Despite that in both applications the conduction losses dominate over the switching and reverse recovery losses.

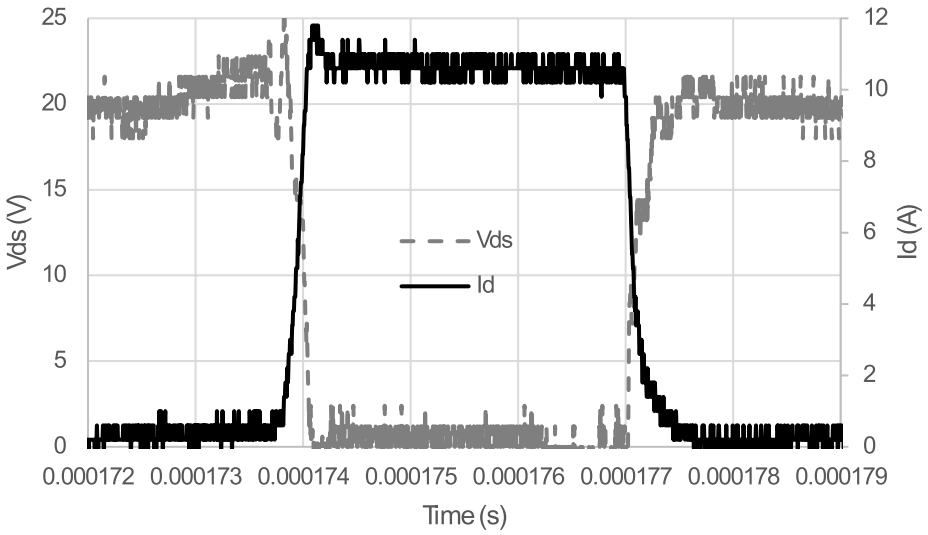

FIGURE 18
V_{ds} and I_D switching waveforms.

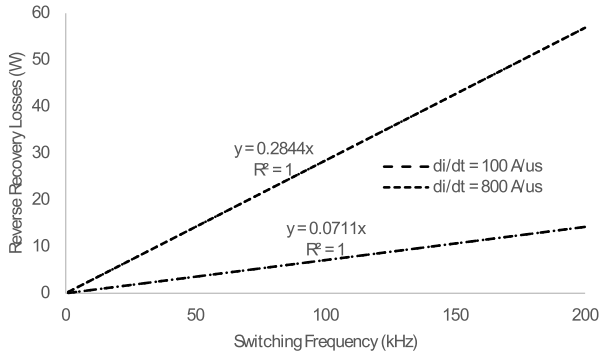

FIGURE 19
Reverse recovery losses.

5 Conclusion

The goal of this work is to examine the performance and efficiency of semiconductor-based protection and compensation systems in low-voltage distribution networks, under both steady-state and disturbed conditions. Two systems are investigated using PSIM simulation tools: 1) a Fault Current Limiting and Interrupting Device (FCLID) based on a Switched Capacitor (SC) circuit, which provides both power factor correction and voltage sag compensation; and 2) a grid-connected photovoltaic (PV) system with energy smoothing, employing a bidirectional DC-DC converter.

A key contribution of this study is the comprehensive comparison of simulation results with theoretical analysis, datasheet values, and industry standards. The PSIM Thermal Module accurately predicts losses within 1% of analytical calculations. It is also shown that lower switching frequencies yield higher overall system efficiency exceeding 96% regardless of specific semiconductor device characteristics (MOSFET or IGBT).

For the FCLID system, tuning the duty cycle and LC values achieves a corrected power factor of 0.85 while maintaining the load voltage within ±5% of the supply voltage. Moreover, the SC circuit can effectively mitigate voltage sags—for instance, correcting a 15.3% drop to within 2.05% of nominal. Switching and conduction losses in the SC system total 42 W per cycle. For the PV system, PSIM offers accurate modelling of switching losses and system efficiency, though inductor losses

TABLE 18 Total power losses for the 4 IGBT.

Datasheet normalization	PSIM simulation	Theory	Practical considerations	%Difference
$P_{cond} + P_{sw}$	$P_{cond} + P_{sw}$	$P_{cond} + P_{sw}$	$P_{cond} + P_{sw}$	
(W)	(W)	(W)	(W)	(%)
4x (0.296 + 8.77)	4x (8.62 + 0.268)	4x (8.77 + 0.213)	4x (10.35 + 0.356)	20.45
4 × 9.066	4 × 8.888	4 × 8.983	4 × 10.706	
36.264	35.552	35.932	42.0824	

TABLE 19 Losses in MPPT.

MPPT PV boost converter P_{Loss} = 40.49W (PSIM Simulation)								MPPT PV boost converter P_{Loss} = 41.41W (practical Considerations)					%Difference
MOSFET				Diode		Inductor		MOSFET				Diode	(%)
Diode		MOSFET						Diode		MOSFET			
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{core}	P_{wind}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
0	0	0.42	8.8	9.4	0.7	1.2	19.97	0.071	9.5	0.5	0.77	9.4	2.28

TABLE 20 Losses in inverter.

Inverter losses 93.5W (PSIM Simulation)				Inverter losses 104.02W (practical Considerations)				% difference
Diodes		MOSFETs		Diodes		MOSFETs		
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	(%)
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
4.02	0	67	20.8	4.02	0.071	79.06	20.871	11.31

TABLE 21 Losses in bidirectional converter.

Battery boost converter PLoss = 85W (PSIM Simulation)								Battery boost converter PLoss = 85.82W (practical Considerations)						%Dif
MOSFET				Diode		Inductor		MOSFET				Diode		
Diode		MOSFET						Diode		MOSFET				(%)
P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{core}	P_{wind}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	P_{cond}	P_{sw}	
(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	(W)	
0	0	2.6	16.5	8	1.7	1.2	55	0	0.07	3.2	16.57	8	1.78	1.0

require calibration via experimental data. The analysis shows that copper (i^2R) losses dominate at higher inductance values, highlighting the importance of low-DCR inductors in efficient designs. However, the study also reveals that reverse recovery losses become negligible compared to conduction losses only at low switching frequencies (<10 kHz) and low current slew rates (di/dt < 100 A/μs). Finally, the analysis demonstrates that practical implementation factors can increase total power losses by up to 21%.

Data availability statement

The raw data supporting the conclusions of this article will be made available by the authors, without undue reservation.

Author contributions

SI: Conceptualization, Data curation, Investigation, Methodology, Software, Writing – original draft, Writing – review and editing. AP: Methodology, Writing – review and editing. NC: Software, Writing – original draft. MC: Writing – review and editing, Validation, Investigation. MD: Methodology, Supervision, Writing – original draft. CM: Investigation, Methodology, Writing – original draft.

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